



SPECTRA 16/26/36
Product Reference Manual

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WARNING

This subassembly has not been tested
to show compliance with new FCC rules
(47 CFR Part 15, subpart J).

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*RETURN INFORMATION REFERENCE SHEET

Chapter One

Introduction

1.1 GENERAL INFORMATION

The SPECTRA 26 is a single board multifunction disk and tape controller for use with Texas Instruments' (TI) 990 series of computers. It is constructed on a single full width board, is TILINE compatible, and interfaces with any combination of four Storage Module Drive (SMD) disk drives and four formatted 1/2" tape drives. Configuration changes, including drive mixing and mapping, can be made by setting the appropriate switches outlined in the Drive Configuration Tables.

The SPECTRA 16 and SPECTRA 36 are depopulated versions of the SPECTRA 26; the SPECTRA 36 is a tape only controller, the SPECTRA 16 a disk only controller.

The SPECTRA 16/26/36 emulates the TI CD1400 and DS80/DS300 disk subsystems, as well as the TI 979 tape subsystem. Emulation is provided for operation with the DX10 operating system.

The SPECTRA 16/26/36 provides high reliability, easy maintainability, and quality performance. Advantages not only include cost savings in the purchase price of the controller, but also the option of buying disk and tape drives from independent manufacturers. Extensive use is made of low-power Schottky and standard Schottky Integrated Circuits on an 8 layer PCB with power and ground planes internal. On board, self-test microdiagnostics execute upon power up, and system level diagnostics allow verification of proper operation on the subsystem. A Light Emitting Diode (LED) indication is provided to aid in fault isolation of the system. Most of the diagnostics run without modification.

The SPECTRA 16/26/36 architecture employs a 2901B processor and a 2911A sequencer using bit slice technology. This design approach provides high performance and flexibility to support most SMD interface compatible disk drives, and Pertec compatible 1/2" interface tape drives. The dual bipolar microprocessor implementation provides simultaneous control of the TILINE interface, disk interface, and tape interface.

1.2 FEATURES

The SPECTRA 16/26/36 controller provides many important features. These features include:

- * Single full width TI compatible PCB.
- * Dual bipolar microprocessor implementation and architecture.
- * Full emulation of the CD1400 disk subsystem.
- * Full emulation of the TI 979 tape subsystem.
- * One model supports any four SMD disk drives.
- * Supports the MT3200 Streamer tape drives.
- * Supports four streaming or formatted start/stop tape drives.
- * Provides an Error Correction Code (ECC) with up to 7-bit burst error correction.
- * Contains 3 sector disk buffering.
- * Supports interleaved and contiguous multiple sector transfers.
- * Supports concurrent 2.0MB/sec disk and 800KB/sec tape data transfers.
- * Automatic Position Verification.
- * Automatic Alternate Track Seeking.
- * Removable or fixed media compatible.
- * Power consumption comparable to disk-only controllers (SPECTRA 26).

1.3 SPECIFICATIONS

FUNCTIONAL CHARACTERISTICS	DISK	TAPE
Drive Attachment	4	4
Interface	All SMD drives	Formatted 1/2"
Base Address	F800-F8F0 (hexadecimal)	F800-F8F0 (hex)
Sector Addressing	Contiguous or Interleaved	N/A
DMA Addressing Range	20 bit	20 bit
DMA Burst Control	1 to 128 words	-----
DMA Block Mode Transfer	Yes	No
Interrupt Priority level	Slot Dependent	Slot Dependent
Buffering	1024 bytes	64 byte FIFO
Capacity/Configuration	Selectable	N/A
Error Correction Code	32-bit ECC Polynomial	N/A
Seek Operation Control	Overlapped	N/A
Transfer Rate	Up to 2.0MB/sec	Up to 800KB/sec

SPECIFICATIONS [continued]

PHYSICAL CHARACTERISTICS	SPECIFICATION
PCB Size	Single full width 10.8"x 14.2"; 8 layers.
Cable Connections	Disk: One 60 pin flat cable connector and four 26 pin flat cable connectors mounted at edge of the PCB. Tape: Two 50 pin flat cable connectors.
Environmental	Exceeds TI 990 temperature and humidity specifications.
Power	+5 volts DC @ 7 amps. -12 volts DC @ .7 amps.

1.4 WARRANTY

Spectra Logic Corporation provides a 12 month limited warranty for the SPECTRA 16/26/36 controller. Repair of PCBs returned in warranty to Spectra Logic will be effected within ten (10) working days after receipt of the failing unit. Repair of PCBs out of warranty will be performed at a nominal charge.

Chapter Two

Installation

2.1 INSTALLATION PROCEDURE

This chapter contains the information needed to install the SPECTRA 16/26/36 controller in any I/O slot of the TI 990 computer. Installation/maintenance personnel should be familiar with both the TI hardware and the specific disk and tape drives being installed. The installation procedure is as follows:

1. Inspect controller board and cables.
2. Configure controller board.
3. Configure drive.
4. Prepare CPU.
5. Install controller board.
6. Connect cables.

2.2 INSPECTION

Perform a thorough visual inspection of the SPECTRA 16/26/36 PCB and cables after removal from their shipping container. Note all damage and notify the freight carrier immediately, as Spectra Logic's warranty does not cover shipping damage. Any damage claim is to be filed through the carrier with its insurance company.

Check for any broken components or bent pins, and ensure that any socketed ICs are securely in place. Inspect the interface cables for cut or broken wires, ensure that the cable is cleanly terminated with the connector.

2.3 CONTROLLER SETUP

The SPECTRA 16/26/36 disk and tape controllers are configured using switches and jumpers. The jumper and switch settings must be set up to the configuration desired before installation into the CPU or expansion chassis.

2.3.1 JUMPER SETTINGS

There are three jumpers on the SPECTRA 16/26/36 controller. In most cases the "standard" setting is with the jumper installed. To select an alternate option, a trace must be cut, or a jumper must be removed or moved to a different location.

Tape Microdiagnostic Enable Jumper (W10)

Jumper W10 enables magnetic tape microdiagnostic routines when installed on the SPECTRA 26/36. If the controller is failing the tape microdiagnostic tests, the jumper may be removed causing the controller to skip these tests and allow the SPECTRA 26 to function as a disk controller only.

W10

IN	Tape microdiagnostics enabled.
OUT	Tape microdiagnostics disabled.

Emulation Select Jumpers (W8, W9)

Jumpers W8 and W9 select the disk drive emulation to be used. These jumpers should not normally be changed; however, if required, contact Spectra Logic.

W8, W9

A 0	<u> </u>	--0 B	Selects Trident emulation (models M and P).
A 0--	<u> </u>	0 B	Selects CD1400 emulation (all other models).

Mag Tape Address Select Jumpers (Location 15L)

The SPECTRA 26/36 has four jumpers installed to control mag tape address selection. The controller is shipped from the factory with the jumpers installed in location 15L in the following configuration.

```

0---0  0  0---0
0---0  0  0---0
1   2  3  4  5

```

In this configuration, each physical unit corresponds to two logical units. Only two physical units (units 0 and 2) may be attached to the controller in this configuration. For streaming tape drives or dual density start/stop drives with remote density select, speed or density is selected by addressing the appropriate logical unit.

LOGICAL UNIT #	PHYSICAL UNIT #	SPEED/DENSITY
0	0	LOW
1	0	HIGH
2	2	LOW
3	2	HIGH

If more than two physical units are to be attached to the controller, the following configuration should be used. Each logical unit corresponds to one physical unit. To select high speed/density remove jumper 4.

LOGICAL UNIT #	PHYSICAL UNIT #	SPEED/DENSITY
0	0	LOW
1	1	LOW
2	2	LOW
3	3	LOW

It may be required to mix a start/stop transport with a streaming transport. This may be accomplished by using the FAD signal with the jumpers changed to the following configuration.

LOGICAL UNIT #	PHYSICAL UNIT #	SPEED/DENSITY
0	0	LOW
1	0	HIGH
2	1	LOW
3	1	HIGH

2.3.2 SWITCH SETTINGS**TILINE Address Switch (Location 3R, SW1-SW8)**

The DIP switch in location 3R establishes the controller's disk and tape address. The disk and tape portions must be assigned to different addresses. The TILINE addresses shown are in hexadecimal.

DISK:	1	2	3	4		<u>TILINE ADDRESS</u>
TAPE:	5	6	7	8		
	OFF	OFF	OFF	OFF		F8F0
	ON	OFF	OFF	OFF		F8E0
	OFF	ON	OFF	OFF		F8D0
	ON	ON	OFF	OFF		F8C0
	OFF	OFF	ON	OFF		F8B0
	ON	OFF	ON	OFF		F8A0
	OFF	ON	ON	OFF		F890
	ON	ON	ON	OFF		F880
	OFF	OFF	OFF	ON		F870
	ON	OFF	OFF	ON		F860
	OFF	ON	OFF	ON		F850
	ON	ON	OFF	ON		F840
	OFF	OFF	ON	ON		F830
	ON	OFF	ON	ON		F820
	OFF	ON	ON	ON		F810
	ON	ON	ON	ON		F800

CPU Option Switch (Location 10P, SW1-SW8)

The DIP switch at location 10P is not used on the M model of the SPECTRA 16. For other models, it provides a burst rate option, a format option, a sector interleave option, and a data chaining option. These options are described below.

Burst Rate Option (Location 10P, SW1, SW2, SW3)

The burst rate is the number of words the controller will transfer on the TILINE interface each time it obtains access to the TILINE during data transfers.

<u>SW1</u>	<u>SW2</u>	<u>SW3</u>	<u>BURST RATE</u>
OFF	OFF	OFF	1 WORD
ON	OFF	OFF	2 WORDS
OFF	ON	OFF	4 WORDS
ON	ON	OFF	8 WORDS
OFF	OFF	ON	16 WORDS
ON	OFF	ON	32 WORDS
OFF	ON	ON	64 WORDS
ON	ON	ON	128 WORDS

<u>TRANSFER RATE</u>	<u>INTERLEAVING</u>	<u>RECOMMENDED BURST RATE</u>
1.2 MB/sec	3:1	1 WORD
1.2 MB/sec	2:1	2 WORDS
1.2 MB/sec	1:1	4 WORDS
1.8 MB/sec	3:1	4 WORDS
1.8 MB/sec	2:1	8 WORDS
1.8 MB/sec	1:1	16 WORDS

Data Chaining Option (Location 10P, SW4)

When this switch is on, data chaining is enabled on the SPECTRA 26, model T. See Appendix A for further information.

SW4

ON	Data chaining enabled.
OFF	Data chaining disabled.

Format Option (Location 10P, SW5)

The format option is generally used when mapping fixed/removable media. To prevent the disk system from selecting the incorrect head on a mapped drive such as this, the SPECTRA 16/26 optionally formats the disk with the physical head number rather than the logical. This ensures that the head addresses are different for the two logical drives. When testing the fixed portion of a CDC, CMD, or Ampex DFR, the diagnostics will report several more errors with this option enabled.

SW5

ON Physical head format.
 OFF Logical head format.

Sector Interleave Option (Location 10P, SW6, SW7, SW8)

Sectors may be interleaved 1:1, 2:1, or 3:1 on the SPECTRA 16/26 controller. For media compatibility, the SPECTRA 16/26 should interleave sectors 3:1. However, 3:1 interleaving is not supported on a drive where the number of sectors per track is exactly divisible by 3. If media compatibility is not an issue, the interleave factor may be changed to 1:1, or 2:1 if the drive has an odd number of sectors. The default value for sector interleaving is set for each drive in the Drive Configuration PROM; for standard configurations the default is 3:1. To change this value, it is necessary to set switches 6, 7, and 8 as given below.

<u>SW6</u>	<u>SW7</u>	<u>SW8</u>	
---	---	OFF	Sector interleave default value is used.
OFF	OFF	ON	3:1 interleave.
ON	OFF	ON	2:1 interleave.
---	ON	ON	1:1 interleave.

Disk Option Switch (Location 17A, SW1-SW4)

The piano switch at location 17A (near the rear edge of the PCB) provides the following options.

System Write Protect (SW1)

When this switch is closed, all writes to the drives attached to the controller will be inhibited. When this switch is open, all writes to the drives are allowed.

SW1
CLOSED Inhibits Write operations.

OPEN (STD) Allows Write operations.

Inhibit ECC Correction (SW2)

When this switch is closed, no attempt will be made to correct ECC errors and data will be written to memory as it was read from the disk. When this switch is open, ECC errors are corrected.

SW2
CLOSED Inhibits ECC corrections.

OPEN (STD) Allows ECC corrections.

Inhibit Format Command (SW3)

When this switch is closed, all FORMAT commands to the drives attached to the controller will be inhibited. When this switch is open, all FORMAT commands are performed.

SW3
CLOSED Inhibits FORMAT commands.

OPEN (STD) FORMAT commands are performed.

Alternate Track Feature (SW4)

When this switch is closed, the Alternate Track Feature is enabled. When this switch is open, the Alternate Track Feature is disabled. For more information, refer to section 3.2.3 (WRITE FORMAT FLAGGED command or RELOCATE command descriptions).

SW4
CLOSED Enables Alternate Track Feature.

OPEN (STD) Disables Alternate Track Feature.

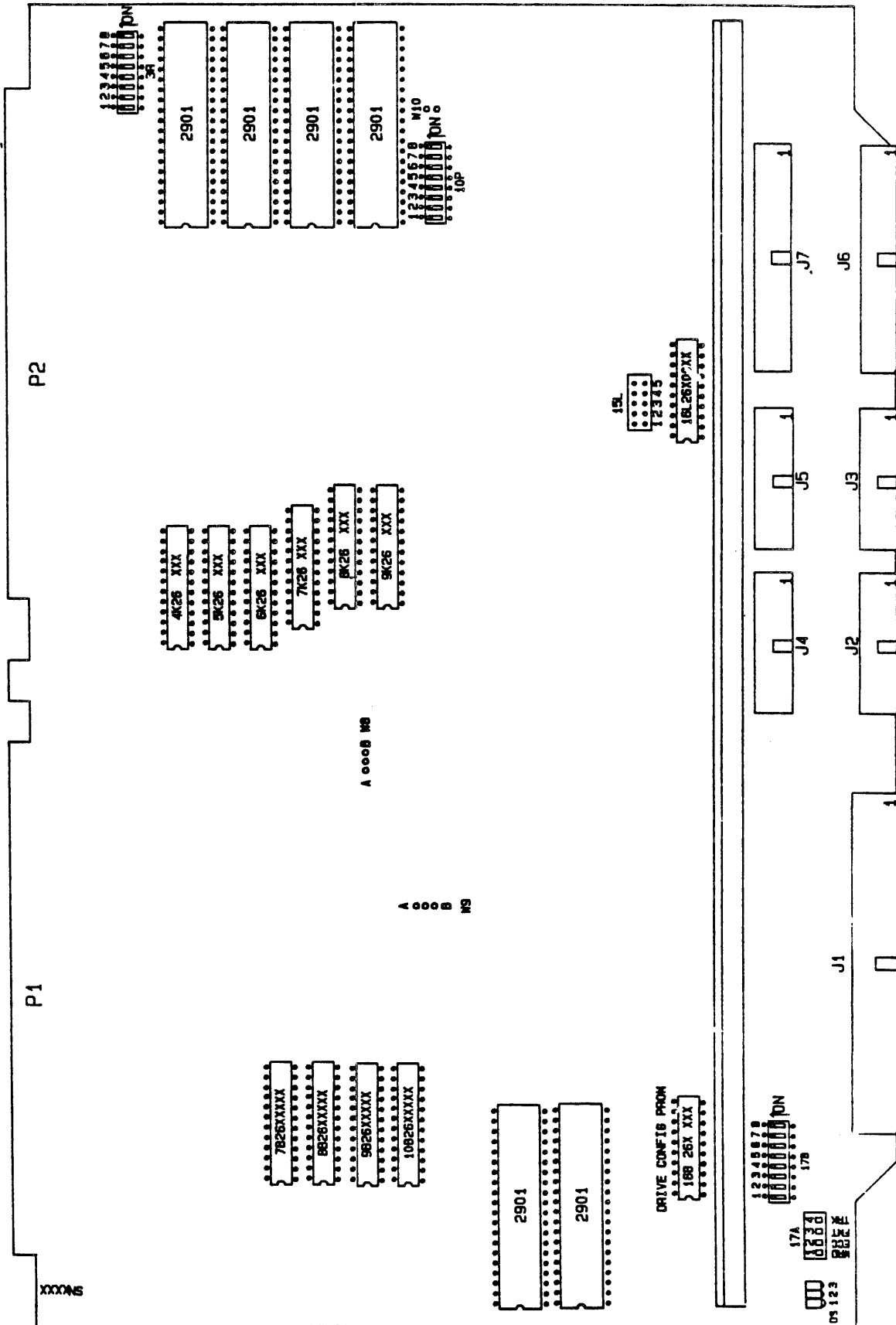


FIG. 2-1 SWITCH/JUMPER LOCATION

2.3.3 DISK DRIVE CONFIGURATION (Location 17B)

Drive configuration for the SPECTRA 16/26 controller is done through the use of a Drive Configuration PROM. The Drive Configuration PROM contains 16 blocks of 32 bytes. A block is selected by the Drive Configuration switches 1-4 in location 17B. Each block of 32 bytes is divided into four sub-blocks of eight bytes; each sub-block defines the parameters of a logical drive allowing a maximum of four logical drives to be attached to the controller. A sub-block is defined as follows:

BLOCK BYTE DEFINITIONS

BYTE 0	The number of logical heads.
BYTE 1	Number of sectors for all drives.
BYTE 2,3	Number of logical cylinders.
BYTE 4	The drive type: Bit 7 = Mapped drive. Bit 6 = CMD type. Bit 5 = CDC Lark type. Bit 4 = Interleaved sectors 3:1. Bit 3 = Interleaved sectors 2:1. Bit 2 = Unused. Bit 1 = Reserved for physical drive number. Bit 0 = Reserved for physical drive number.
BYTE 5	Head offset.
BYTE 6	Mapped cylinders (bit 7).
BYTE 6 bits 6-3	Number of alternate cylinders. This four bit number is multiplied by 2 to give any even number from 0-30.
BYTE 6 bits 2-0	Cylinder offset (if cylinders are mapped).
BYTE 7	Cylinder offset (if cylinders are mapped).

DISK DRIVE CONFIGURATION TABLES

The following tables list the drives to which the SPECTRA 16/26/36 controllers interface and the versions which support them.

AMPEX						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
DM940	40MB	411	5	64	A	
DM980	80MB	823	5	61,64	A,B,C	
DM980	80MB	823	5	56	M	
DM9160	160MB	1645	5	64	B	
DM9300	300MB	815	19	61	A,B,C	
DM9300A	300MB	823	19	61,64	A,B,C	
DM9300A	300MB	823	19	56	M	
C330	330MB	1024	16	64	B	
DFR932	16/16MB	823	1	64	A	2 Logical drives
	16/16MB	823	1	56	M	2 Logical drives
DFR964	16/48MB	823	1	64	A	2 or 4 Logical drives
	16/48MB	823	3	56	M	2 or 4 Logical drives
DFR996	16/80MB	823	1	64	A	2 Logical drives
	16/80MB	823	5	56	M	2 Logical drives

BALL						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
BD160	160MB	1645	5	64	B	

CENTURY DATA SYSTEMS						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
T82	80MB	815	5	61,64	A,B,C,E	
T82	80MB	815	5	56	M	
T302	300MB	815	19	61,64	A,B,C,N	
T302	300MB	815	19	56	M	
M80	80MB	569	6	76	C	
M160	162MB	845	6	101	C	
AMS190	191MB	569	14	76	C	
AMS380	378MB	845	14	101	C	
AMS315	315MB	823	19	61,64	A,B,C	
AMS315	315MB	823	19	56	M	
AMS513	513MB	845	19	101	C	
AMS571	571MB	941	19	104	E	

DISK DRIVE CONFIGURATION TABLES

CONTROL DATA CORPORATION						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
9760	40MB	411	5	64	A	
9762	80MB	823	5	61,64	A,B,C,E	
9762	80MB	823	5	56	M	
9766	300MB	823	19	61,64	A,B,C,N,E	
9766	300MB	823	19	56	M	
9448-32	16/16MB	823	2	64	A	2 Logical drives
	16/16MB	823	2	56	M	2 Logical drives
9448-64	16/48MB	823	4	64	A	2 or 4 Logical drives
	16/48MB	823	4	56	M	2 or 4 Logical drives
9448-96	16/80MB	823	6	64	A	2 Logical drives
	16/80MB	823	6	56	M	2 Logical drives
9730-80	80MB	823	5	61,64	A,B,C,E	
9730-80	80MB	823	5	56	M	
9730-160	160MB	823	10	64	B,D,N	
9730-160	160MB	823	10	61,64	B,D	2 X 80
9730-160	160MB	823	10	56	M	
9730-160	160MB	823	10	56	M	2 X 80
9775	675MB	843	40	61	B,F	2 X 300
9455-16	8/8MB	206	4	64	A	2 Logical drives
9455-50	25/25MB	624	2	64	A,D	2 Logical drives
9710	80MB	823	5	61,64	A,B,C,E	
9710	80MB	823	5	56	M	
9715-160	160MB	823	10	64	B,D,N	
9715-160	160MB	823	10	61,64	B,D	2 X 80
9715-160	160MB	823	10	56	M	
9715-160	160MB	823	10	56	M	2 X 80
9715-340	340MB	711	24	64	N	
9715-500	500MB	711	24	95	N,E	
9771	825MB	1024	16	128	D	
9412	80MB	784	5	64	D	
9720	368MB	1217	10	95	F	

DISC TECH ONE						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
4300	300MB	832	14	82	D	

DISK DRIVE CONFIGURATION TABLES

FUJITSU						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
2211	80MB	823	5	61,64	A,B,C,E	
2211	80MB	823	5	56	M	
2312	84MB	589	7	64	A,B,C,D,E,N,F	
2312	84MB	589	7	56	M	
2284	165MB	823	10	64	B,D	
2284	165MB	823	10	61,64	B,D	2 X 80
2284	165MB	823	10	56	M	
2284	165MB	823	10	56	M	2 X 80
2294	330MB	1024	16	64	B	
2298	671MB	1024	16	130	E	
2351	474MB	842	20	88	B,E,D	2x235 & 1x474
*2322	165MB	823	10	56,61,64	B,D,M,N,P	

*When running 64 sectors/track, set byte/sector count on the drive to 319, which is ONE BYTE LESS than the drive chart shows for 64 sectors.

KENNEDY						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
5380	80MB	823	5	61,64	A,B,C,E	
5380	80MB	823	5	56	M	
53160	160MB	823	10	64	B,D	
53160	160MB	823	10	61,64	B,D	2 X 80
7340	340MB	411	5	64	A	
7380	380MB	823	5	61,64	A,B,C,E	

NEC						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
2268	337MB	823	10	128	F	2 X 168.5 & 1 X 337
2352	520MB	760	19	113	F	2 X 260 & 1 X 520

DISK DRIVE CONFIGURATION TABLES

PRIAM						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
3350	34MB	561	3	64	C	
3350	34MB	561	3	56	M	
6650	67MB	1121	3	64	C	
6650	67MB	1121	3	56	M	
15450	155MB	1121	7	64	C	
15450	155MB	1121	7	56	M	
3450	35MB	525	5	43	C	
7050	70MB	1049	5	43	C	
803	85MB	850	5	64	F	
804	100MB	1050	5	64	F	
806	188MB	850	11	64	F	
807	344MB	1552	11	64	F	
808	516MB	1552	11	96	F	
806	266MB	1023	11	64	F	

TECSTOR						
MODEL #	CAPACITY	CYLS	HDS	SECS	VERSION	MAPPING
160	160MB	704	12	64	C	
166	166MB	823	10	61,64	B,D	2 X 80
166	166MB	823	10	64	B,D	
315	315MB	823	19	61,64	A,B,C	
315	315MB	823	19	56	M	

S16/26 MODEL ADRIVE CONFIGURATION TABLE
VERSION A4

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/64	(FUJITSU)
1	ON	ON	ON	OFF	0,1,2	0,1,2	80MB SMD	823/5/64	
					3	3	300MB SMD	823/19/64	
2	ON	ON	OFF	ON	0,1,2,3	0,1,2,3	300MB SMD	823/19/64	
					0,1,2	0,1,2	80MB SMD	815/5/61	
3	ON	ON	OFF	OFF	3	3	300MB SMD	815/19/61	
					0,1,2	0,1,2	300MB SMD	815/19/61	
4	ON	OFF	ON	ON	3	3	80MB SMD	815/5/61	
					0,2	0,2	16MB CMD/DFR	823/1/64	REMOVABLE
5	ON	OFF	ON	OFF	1,3	0,2	16MB CMD/DFR	823/1/64	FIXED
					0,2	0,2	16MB CMD/DFR	823/1/64	FIXED
6	ON	OFF	OFF	ON	1,3	0,2	16MB CMD/DFR	823/1/64	REMOVABLE
					0,2	0,2	16MB CMD/DFR	823/1/64	REMOVABLE
7	ON	OFF	OFF	OFF	1,3	0,2	48MB CMD/DFR	823/3/64	FIXED
					0,2	0,2	16MB CMD/DFR	823/1/64	REMOVABLE

S16/26 MODEL ADRIVE CONFIGURATION TABLE
VERSION A4

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,2	0,2	48MB CMD/DFR	823/3/64	FIXED
					1,3	0,2	16MB CMD/DFR	823/1/64	REMOVABLE
9	OFF	ON	ON	OFF	0,2	0,2	16MB CMD/DFR	823/1/64	REMOVABLE
					1,3	0,2	80MB CMD/DFR	823/5/64	FIXED
10	OFF	ON	OFF	ON	0,2	0,2	80MB CMD/DFR	823/5/64	FIXED
					1,3	0,2	16MB CMD/DFR	823/1/64	REMOVABLE
11	OFF	ON	OFF	OFF	0,1,2,3	0	16MB CMD/DFR	823/1/64	0=REMOVABLE 1=FIXED HEAD 0 2=FIXED HEAD 1 3=FIXED HEAD 2
					0,1,2,3	0	16MB CMD/DFR	823/1/64	0=FIXED HEAD 0 1=REMOVABLE 2=FIXED HEAD 1 3=FIXED HEAD 2
13	OFF	OFF	ON	OFF	0,2	0,2	8MB LARK I	206/2/64	FIXED
					1,3	0,2	8MB LARK I	206/2/64	REMOVABLE
14	OFF	OFF	ON	OFF	0,2	0,2	25MB LARK II	624/2/64	FIXED
					1,3	0,2	25MB LARK II	624/2/64	REMOVABLE
15	OFF	OFF	OFF	OFF	0,1,2,3	0,1,2,3	40MB SMD	411/5/64	

STORE REGISTER VALUES VERSION A4

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0,1,2 3	2000 2000	4000 4000	2B2B 9B2B	2B35 9B35	80MB SMD 300MB SMD
2	0,1,2,3	2000	4000	9B2B	9B35	300MB SMD
3	0,1,2 3	1E80 1E80	3D00 3D00	2B23 9B23	2B23 9B23	80MB SMD 300MB SMD
4	0,1,2 3	1E80 1E80	3D00 3D00	9B23 2B23	9B23 2B23	300MB SMD 80MB SMD
5	0,1,2,3	2000	4000	0B2B	0B35	16MB CMD/DFR
6	0,1,2,3	2000	4000	0B2B	0B35	16MB CMD/DFR
7	0,2 1,3	2000 2000	4000 4000	0B2B 1B2B	0B35 1B35	16MB CMD/DFR 48MB CMD/DFR
8	0,2 1,3	2000 2000	4000 4000	1B2B 0B2B	1B35 0B35	48MB CMD/DFR 16MB CMD/DFR
9	0,2 1,3	2000 2000	4000 4000	0B2B 2B2B	0B35 2B35	16MB CMD/DFR 80MB CMD/DFR
10	0,2 1,3	2000 2000	4000 4000	2B2B 0B2B	2B35 0B35	80MB CMD/DFR 16MB CMD/DFR
11	0,1,2,3	2000	4000	0B2B	0B35	16MB CMD/DFR
12	0,1,2,3	2000	4000	0B2B	0B35	16MB CMD/DFR
13	0,1,2,3	2000	4000	10C2	10CC	8MB LARK I
14	0,1,2,3	2000	4000	1264	126E	25MB LARK II
15	0,1,2,3	2000	4000	298F	2999	40MB SMD

S16/26 MODEL BDRIVE CONFIGURATION TABLE
VERSION B2

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/64	(FUJITSU)
1	ON	ON	ON	OFF	0,1,2	0,1,2	80MB SMD	823/5/64	
					3	3	300MB SMD	823/19/64	
2	ON	ON	OFF	ON	0,1,2	0,1,2	300MB SMD	823/19/64	
					3	3	80MB SMD	823/5/64	
3	ON	ON	OFF	OFF	0,1,2	0,1,2	80MB SMD	815/5/61	
					3	3	300MB SMD	815/19/61	
4	ON	OFF	ON	ON	0,1,2	0,1,2	300MB SMD	815/19/61	
					3	3	80MB SMD	815/5/61	
5	ON	OFF	ON	OFF	0,1,2,3	0,1,2,3	160MB MMD	823/10/64*	
6	ON	OFF	OFF	ON	0,2	0,2	160MB MMD	823/10/64	HEADS 0-4
					1,3	0,2	160MB MMD	823/10/64	HEADS 5-9
7	ON	OFF	OFF	OFF	0,2	0,2	160MB MMD	815/10/61	HEADS 0-4
					1,3	0,2	160MB MMD	815/10/61	HEADS 5-9

*When using a Fujitsu 2322-168 Mbyte drive for any of the 160 Mbyte drive types, the drive **MUST** be set as follows:

- Use 64 sectors/track.
- Set byte/sector count to 319.

(NOTE: This is **ONE BYTE LESS** than the drive chart indicates for 64 sectors).
which is **ONE BYTE LESS** than the drive chart shows for 64 sectors.

S16/26 MODEL BDRIVE CONFIGURATION TABLE
VERSION B2

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,1	0	FUJITSU 160MB SMD	815/10/61	0=HEADS 0-4 1=HEADS 5-9
					2,3	2,3	80MB SMD	815/5/61	
9	OFF	ON	ON	OFF	0,3	0,3	80MB SMD	815/5/61	
					1,2	1	160MB SMD	815/10/61	1=HEADS 0-4 2=HEADS 5-9
10	OFF	ON	OFF	ON	0,1	0	675MB STD	815/40/61	0=HEADS 0-18 1=HEADS 19-37
					2,3	2,3	300MB SMD	815/19/61	
11	OFF	ON	OFF	OFF	0,3	0,3	300MB SMD	815/19/61	
					1,2	1	675MB STD	815/40/61	1=HEADS 0-18 2=HEADS 19-37
12	OFF	OFF	ON	ON	0,1	0	EAGLE 474MB 2351	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2	EAGLE 474MB 2351	842/20/88	2=HEADS 0-9 3=HEADS 10-19
13	OFF	OFF	ON	OFF	0,1,2,3	0,1,2,3	AMPEX 330MB C330	1024/16/64	
14	OFF	OFF	OFF	ON	0,1,2,3	0,1,2,3	160MB STD	1643/5/64	
15	OFF	OFF	OFF	OFF	0,1	0	474MB 2351	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2,3	300MB SMD	823/19/64	

STORE REGISTER VALUES VERSION B2

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0,1,2 3	2000 2000	4000 4000	2B2B 9B2B	2B35 9B35	80MB SMD 300MB SMD
2	0,1,2 3	2000 2000	4000 4000	9B2B 9B2B	9B35 2B35	300MB SMD 80MB SMD
3	0,1,2 3	1E80 1E80	3D00 3D00	2B23 9B23	2B23 9B23	80MB SMD 300MB SMD
4	0,1,2 3	1E80 1E80	3D00 3D00	9B23 2B23	9B23 2B23	300MB SMD 80MB SMD
5	0,1,2,3	2000	4000	532B	5335	160MB STD
6	0,1,2,3	2000	4000	2B2B	2B35	80MB SMD
7	0,1,2,3	1E80	3D00	2B23	2B23	80MB SMD
8	0,1,2,3	1E80	3D00	2B23	2B23	80MB SMD
9	0,1,2,3	1E80	3D00	2B23	2B23	80MB SMD
10	0,1,2,3	1E80	3D00	9B23	9B23	300MB SMD
11	0,1,2,3	1E80	3D00	9B23	9B23	300MB SMD
12	0,1,2,3	2C00	5800	533E	5348	474MB EAGLE
13	0,1,2,3	2000	4000	83F4	83FE	330MB AMPEX
14	0,1,2,3	2000	4000	2E61	2E6B	160MB STD
15	0,1 2,3	2C00 2000	5800 4000	533E 9B2B	5348 9B35	474MB 2351 300MB SMD

S16/26 MODEL CDRIVE CONFIGURATION TABLE
VERSION C3

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/64	(FUJITSU)
					0,1,2	0,1,2	80MB SMD	823/5/64	
1	ON	ON	ON	OFF	3	3	300MB SMD	823/19/64	
2	ON	ON	OFF	ON	0,1,2,3	0,1,2,3	300MB SMD	823/19/64	
					0,1,2	0,1,2	80MB SMD	815/5/61	
3	ON	ON	OFF	OFF	3	3	300MB SMD	815/19/61	
4	ON	OFF	ON	ON	0,1,2,3	0,1,2,3	300MB SMD	815/19/61	
5	ON	OFF	ON	OFF	0,1,2,3	0,1,2,3	80MB M80	589/6/76	
6	ON	OFF	OFF	ON	0,1,2,3	0,1,2,3	160MB M160	845/6/101	
7	ON	OFF	OFF	OFF	0,1,2,3	0,1,2,3	190MB AMS190	569/14/76	
8	OFF	ON	ON	ON	0,1,2,3	0,1,2,3	380MB AMS380	845/14/101	
9	OFF	ON	ON	OFF	0,1,2,3	0,1,2,3	34MB PRIAM	561/3/64	
10	OFF	ON	OFF	ON	0,1,2,3	0,1,2,3	67MB PRIAM	1121/3/64	
11	OFF	ON	OFF	OFF	0,1,2,3	0,1,2,3	155MB PRIAM	1121/7/64	
12	OFF	OFF	ON	ON	0,1,2,3	0,1,2,3	35MB PRIAM	525/5/43	
13	OFF	OFF	ON	OFF	0,1,2,3	0,1,2,3	70MB PRIAM	1049/5/43	
14	OFF	OFF	ON	OFF	0,1,2,3	0,1,2,3	160MB TECSTOR	704/12/64	
15	OFF	OFF	OFF	OFF	0,1,2,3	0,1,2,3	513MB AMS513	845/19/101	

STORE REGISTER VALUES VERSION C3

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0,1,2 3	2000 2000	4000 4000	2B2B 9B2B	2B35 9B35	80MB SMD 300MB SMD
2	0,1,2,3	2000	4000	9B2B	9B35	300MB SMD
3	0,1,2 3	1E80 1E80	3D00 3D00	2B23 9B23	2B23 9B23	80MB SMD 300MB SMD
4	0,1,2,3	1E80	3D00	9B23	9B23	300MB SMD
5	0,1,2,3	2600	4C00	3224	322E	80MB M80
6	0,1,2,3	3280	6500	3339	3343	160MB M160
7	0,1,2,3	2600	4C00	722D	7237	190MB AMS190
8	0,1,2,3	3280	6500	7341	734B	380MB AMS380
9	0,1,2,3	2000	4000	1A25	1A2F	34MB PRIAM 3350
10	0,1,2,3	2000	4000	1C55	1C5F	67MB PRIAM 6650
11	0,1,2,3	2000	4000	3C55	3C5F	155MB PRIAM 15450
12	0,1,2,3	1580	2B00	2A01	2A0B	35MB PRIAM 3450
13	0,1,2,3	1580	2B00	2C0D	2C17	70MB PRIAM 7050
14	0,1,2,3	2000	4000	62B0	62BA	160MB TECSTOR
15	0,1,2,3	3280	6500	9B41	9B4B	513MB AMS513

S16/26 MODEL DDRIVE CONFIGURATION TABLE
VERSION D5

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB FUJITSU	589/7/64	
1	ON	ON	ON	OFF	0,1	0	25MB 9457 (CDC)	624/2/64	0=FIXED 1=REMOVABLE
					2,3	2,3	80MB 9412	784/5/64	(CDC)
2	ON	ON	OFF	ON	0,1	0	25MB 9457 (CDC)	624/2/64	0=REMOVABLE 1=FIXED
					2,3	2,3	80MB 9412	784/5/64	(CDC WINDSOR)
3	ON	ON	OFF	OFF	0,1	0	160MB STD	823/10/64	0=HEADS 0-4 1=HEADS 5-9
					2,3	2,3	160MB MMD	823/10/64	
4	ON	OFF	ON	ON	0,1,2,3	0,1,2,3	825MB 9771	1024/16/128	(CDC XMD)
					0,2	0,2	80MB SMD	823/5/64	
5	ON	OFF	ON	OFF	1	1	160MB 9715	823/10/64	(CDC FSD I)
					3	3	340MB	711/24/64	(CDC FSD II)
					0,2	0,2	80MB SMD	823/5/64	
6	ON	OFF	OFF	ON	1	1	500MB 9715	711/24/95	(CDC FSD II)
					3	3	825MB 9771	1024/16/128	(CDC XMD)
7	ON	OFF	OFF	OFF	0,1,2	0,1,2	160MB 9715	823/10/64	(CDC FSD I)
					3	3	340MB 9715	711/24/64	(CDC FSD IB)

NOTE: When using a Fujitsu 2322-168 Mbyte drive for any of the 160 Mbyte drive types, the drive MUST be set as follows:

- Use 64 sectors/track.
- Set byte/sector count to 319.

(NOTE: This is ONE BYTE LESS than the drive chart indicates for 64 sectors).

S16/26 MODEL DDRIVE CONFIGURATION TABLE
VERSION D5

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8					0,2	0,2	160MB 9715	823/10/64	(CDC FSD I)
	OFF	ON	ON	ON	1	1	500MB 9715	711/24/95	(CDC FSD II)
					3	3	825MB 9771	1024/16/128	(CDC XMD)
9	OFF	ON	ON	OFF	0,1,2	0,1,2	340MB 9715	711/24/64	(CDC FSD IB)
					3	3	500MB 9715	711/24/95	(CDC FSD II)
10					0	0	340MB 9715	711/24/64	(CDC FSD IB)
	OFF	ON	OFF	ON	1	1	825MB 9771	1024/16/128	(CDC XMD)
					2,3	2,3	500MB 9715	711/24/95	(CDC FSD II)
11	OFF	ON	OFF	OFF	0	0	500MB 9715	711/24/95	(CDC FSD II)
					1,2,3	1,2,3	825MB 9771	1024/16/128	(CDC XMD)
12	OFF	OFF	ON	ON	0,1,2,3	0,1,2,3	300MB 4300	832/14/82	(DISC TECH I)
13	OFF	OFF	ON	OFF	0,1,2,3	0,1,2,3	85MB 803	850/5/64	(PRIAM)
14	OFF	OFF	OFF	ON	0,2	0,2	825MB 9771	1024/16/160	HDS 0 - 7
					1,3	0,2	825MB 9771	1024/16/160	HDS 8 - 15
15	OFF	OFF	OFF	OFF	0	0			(EAGLE)
					1	0	474MB	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2,3	160MB 9715	823/10/64	(CDC FSD 1)

STORE REGISTER VALUES VERSION D5

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0,1 2,3	2000	4000	1264	126E	25MB CDC 9457
		2000	4000	2B04	2BOE	80MB CDC 9412
2	0,1 2,3	2000	4000	1264	126E	25MB CDC 9457
		2000	4000	2B04	2BOE	80MB CDC 9412
3	0,1 2,3	2000	4000	2B2B	2B35	80MB SMD
		2000	4000	532B	5335	160MB MMD
4	0,1,2,3	4000	8000	83F4	83FE	825MB 9771
5	0,2 1 3	2000	4000	2B2B	2B35	80MB SMD
		2000	4000	532B	5335	160MB 9715-160
		2000	4000	C2BB	C2C5	340MB 9715-340
6	0,2 1 3	2000	4000	2B2B	2B35	80MB SMD
		2F80	5F00	C2BB	C2C5	500MB 9715-500
		4000	8000	83F4	83FE	825MB 9771
7	0,1,2 3	2000	4000	532B	5335	160MB MMD
		2000	4000	C2BB	C2C5	340MB 9715-340
8	0,2 1 3	2000	4000	532B	5335	160MB MMD
		2F80	5F00	C2BB	C2C5	500MB 9715-500
		4000	8000	83F4	83FE	825MB 9771
9	0,1,2 3	2000	4000	C2BB	C2C5	340MB 9715-340
		2F80	5F00	C2BB	C2C5	500MB 9715-500
10	0 1 2,3	2000	4000	C2BB	C2C5	340MB 9715-340
		4000	8000	83F4	83FE	825MB 9771
		2F80	5F00	C2BB	C2C5	500MB 9715-500
11	0 1,2,3	2F80	5F00	C2BB	C2C5	500MB 9715-500
		4000	8000	83F4	83FE	825MB 9771
12	0,1,2,3	2900	5200	7334	733E	300MB 4300
13	0,1,2,3	2000	4000	2B46	2B50	85MB 803
14	0,2 1,3	5000	A000	43F4	43FE	820MB CDC XMD
		5000	A000	43F4	43FE	820MB CDC XMD
15	0,1 2,3	2C00	5800	533E	5348	475MB EAGLE
		2000	4000	532B	5335	160MB 9715-160

S16/26 MODEL EDRIVE CONFIGURATION TABLE
VERSION E7

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/64	(FUJITSU)
1	ON	ON	ON	OFF	0,1	0	80MB CMD/DFR 16MB CMD/DFR	823/5/64 823/1/64	FIXED REMOVABLE
					2,3	2,3	80MB SMD	815/5/61	
2	ON	ON	OFF	ON	0,1	0	80MB CMD/DFR 16MB CMD/DFR	823/5/64 823/1/64	FIXED REMOVABLE
					2,3	2,3	300MB SMD	815/19/61	
3	ON	ON	OFF	OFF	0,1	0	474MB 2351	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2	80MB CMD/DFR 16MB CMD/DFR	823/5/64 823/1/64	FIXED REMOVABLE
4	ON	OFF	ON	ON	0,1	0	80MB CMD/DFR 16MB CMD/DFR	823/5/64 823/1/64	FIXED REMOVABLE
					2,3	2	474MB 2351	842/20/88	2=HEADS 0-9 3=HEADS 10-19
5	ON	OFF	ON	OFF	0,1	0	474MB 2351	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2,3	84MB 2312	589/7/64	(FUJITSU)
6	ON	OFF	OFF	ON	0,1,2,3	0,1,2,3	500MB 9715	711/24/95	(CDC FSD II)
					0,1	0	500MB 9715	711/24/95	0=HEADS 0-11 1=HEADS 12-23
7	ON	OFF	OFF	OFF	0,1	0	500MB 9715	711/24/95	0=HEADS 0-11 1=HEADS 12-23
					2,3	2	500MB 9715	711/24/95	2=HEADS 0-11 3=HEADS 12-23

S16/26 MODEL EDRIVE CONFIGURATION TABLE
VERSION E7

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,2	0,1	AMS571	941/19/109	CYLS 0 - 468
					1,3	0,1	AMS571	941/19/109	CYLS 470-938
9	OFF	ON	ON	OFF	0,1,2,3	0,1,2,3	FUJI 2298	1024/16/130	
10	OFF	ON	OFF	ON	0,1,2,3	0,1,2,3	PERTEC 300MB	1493/10/64	
11	OFF	ON	OFF	OFF	0,1,2,3	0,1,2,3	NT 225MB	1029/10/66	
12	OFF	OFF	ON	ON	0,1,2,3	0,1,2,3	474MB 2351	842/20/88	ONE PHYSICAL ONE LOGICAL UNIT
13	OFF	OFF	ON	OFF	NOT USED				
14	OFF	OFF	OFF	ON	NOT USED				
15	OFF	OFF	OFF	OFF	NOT USED				

STORE REGISTER VALUES VERSION E7

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0	2000	4000	2B2B	2B35	80MB CMD/DFR
	1	2000	4000	0B2B	0B35	16MB CMD/DFR
	2,3	1E80	3D00	2B23	2B23	80MB SMD
2	0	2000	4000	2B2B	2B35	80MB CMD/DFR
	1	2000	4000	0B2B	0B35	16MB CMD/DFR
	2,3	1E80	3D00	9B23	9B23	300MB SMD
3	0,1	2C00	5800	533E	5348	474MB 2351
	2	2000	4000	2B2B	2B35	80MB CMD/DFR
	3	2000	4000	0B2B	0B35	16MB CMD/DFR
4	0	2000	4000	2B2B	2B35	80MB CMD/DFR
	1	2000	4000	0B2B	0B35	16MB CMD/DFR
	2,3	2C00	5800	533E	5348	474MB 2351
5	0,1	2C00	5800	533E	5348	474MB 2351
	2,3	2000	4000	3A41	3A4B	84MB FUJITSU
6	0,1,2,3	2F80	5F00	C2BB	C2C5	500MB 9715-500
7	0,1,2,3	2F80	5F00	62BB	62C5	500MB 9715-500
8	0,1,2,3	3400	6800	99CA	99D4	571MB AMS571
9	0,1,2,3	4100	8200	83F4	83FE	670MB FUJI 2298
10	0,1,2,3	2000	4000	55C9	55D3	300MB, PERTEC
11	0,1,2,3	2100	4200	53F9	5403	225MB, NT
12	0,1,2,3	2C00	5800	A33E	A348	474MB 2351
13	0,1,2,3			NOT USED		
14	0,1,2,3			NOT USED		
15	0,1,2,3			NOT USED		

S16/26 MODEL FDRIVE CONFIGURATION TABLE
VERSION F5

	4 3 2 1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON ON ON ON	0,1,2,3	0,1,2,3	FUJI 2312	589/7/64	84MB
1	ON ON ON OFF	0,2	0	PRIAM 803	850/5/64	85MB
		1,3	1	PRIAM 806	850/11/64	188MB
2	ON ON OFF ON	0,1,2,3	0,1,2,3	PRIAM 804	1050/5/64	100MB
3	ON ON OFF OFF	0,1,2,3	0,1,2,3	PRIAM 806	850/11/64	188MB
4	ON OFF ON ON	0,1,2,3	0,1,2,3	PRIAM 807	1552/11/64	344MB
5	ON OFF ON OFF	0,1,2,3	0,1,2,3	PRIAM 808	1552/11/96	516MB
6	ON OFF OFF ON	0,1,2,3	0,1,2,3	CDC 9720	1217/10/95	368MB
7	ON OFF OFF OFF	0,1	0,1	CDC 9720	1217/10/95	368MB
		2	2	300MB SMD	823/19/64	
		3	3	80MB SMD	823/5/64	
8	OFF ON ON ON	0,1,2	0,1,2	CDC 9720	1217/10/95	368MB
		3	3	160MB SMD	823/10/64	
9	OFF ON ON OFF	0,1	0	CDC 9775	843/40/64	0=HEADS 0-19 1=HEADS 20-40
		2,3	2	CDC 9775	843/40/64	2=HEADS 0-19 3=HEADS 20-40
10	OFF ON OFF ON	0,1,2,3	0,1,2,3	PRIAM 806-23	1023/11/64	266MB
11	OFF ON OFF OFF	0,1	0,1	NEC 2268	823/10/128	337MB
		2,3	2	NEC 2352	380/19/113	2=CYLS 0-379 3=CYLS 380-759
12	OFF OFF ON ON	0,1	0,1	NEC 2268	823/10/128	337MB
		2,3	2,3	NEC 2352	760/19/113	520MB
13	OFF OFF ON OFF	0,1	0	NEC 2268	823/5/128	0=HEADS 0-4 1=HEADS 5-9
		2,3	2	NEC 2352	380/19/113	2=CYLS 0-379 3=CYLS 380-759
14	OFF OFF OFF ON	NOT USED				
15	OFF OFF OFF OFF	NOT USED				

STORE VERSION VALUES VERSION F5

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	FUJI 2312
1	0,2 1,3	2000	4000	2B46	2B50	PRIAM 803
		2000	4000	5B46	5B50	PRIAM 806
2	0,1,2,3	2000	4000	2COE	2C18	PRIAM 804
3	0,1,2,3	2000	4000	5B46	5B50	PRIAM 806
4	0,1,2,3	2000	4000	5E04	5EOE	PRIAM 807
5	0,1,2,3	3000	6000	5E04	5EOE	PRIAM 808
6	0,1,2,3	2F80	5F00	54B5	54BF	CDC 9720
7	0,1 2 3	2F80	5F00	54B5	54BF	CDC 9720
		IE80	3D00	9B2B	9B35	300MB SMD
		IE80	3D00	2B2B	2B35	80MB SMD
8	0,1,2 3	2F80	5F00	54B5	54BF	CDC 9720
		2000	4000	532B	5335	160MB SMD
9	0,1,2,3	2000	4000	A33F	A349	CDC 9775
10	0,1,2,3	2000	4000	5BF3	5BFD	PRIAM 806-23
11	0,1 2,3	4000	8000	532B	5335	NEC 2268
		3880	7100	9970	997A	NEC 2352
12	0,1 2,3	4000	8000	532B	5335	NEC 2268
		3880	7100	9AEC	9AF6	NEC 2352
13	0,1 2,3	4000	8000	2B2B	2B35	NEC 2268
		3880	7100	9970	997A	NEC 2352
14		NOT USED				
15		NOT USED				

S16/26 MODEL MDRIVE CONFIGURATION TABLE
VERSION M1

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/56	(FUJITSU)
1	ON	ON	ON	OFF	0,1,2	0,1,2	80MB SMD	823/5/56	
					3	3	300MB SMD	823/19/56	
2	ON	ON	OFF	ON	0,1,2	0,1,2	300MB SMD	823/19/56	
					3	3	80MB SMD	823/5/56	
3	ON	ON	OFF	OFF	0,1,2	0,1,2	160MB MMD	823/10/56	
					3	3	300MB SMD	823/19/56	
4	ON	OFF	ON	ON	0,1	0	160MB MMD	823/10/56	0=HEADS 0-4 1=HEADS 5-9
					2,3	2,3	80MB SMD	823/5/56	
5	ON	OFF	ON	ON	0,1	0	16MB CMD 16MB CMD	823/1/56 823/1/56	0=REMOVABLE 1=FIXED
					2,3	2	16MB CMD 16MB CMD	823/1/56 823/1/56	2=REMOVABLE 3=FIXED
6	ON	OFF	OFF	ON	0,1	0	16MB CMD 16MB CMD	823/1/56 823/1/56	0=FIXED 1=REMOVABLE
					2,3	2	16MB CMD 16MB CMD	823/1/56 823/1/56	2=FIXED 3=REMOVABLE
7	ON	OFF	OFF	OFF	0,1	0	16MB CMD 48MB CMD	823/1/56 823/3/56	0=REMOVABLE 1=FIXED
					2,3	2	16MB CMD 48MB CMD	823/1/56 823/3/56	2=REMOVABLE 3=FIXED

S16/26 MODEL MDRIVE CONFIGURATION TABLE
VERSION M1

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,1	0	48MB CMD 16MB CMD	823/3/56 823/1/56	0=FIXED 1=REMOVABLE
					2,3	2	48MB CMD 16MB CMD	823/3/56 823/1/56	2=FIXED 3=REMOVABLE
9	OFF	ON	ON	OFF	0,1	0	16MB CMD 80MB CMD	823/1/56 823/5/56	0=REMOVABLE 1=FIXED
					2,3	2	16MB CMD 80MB CMD	823/1/56 823/5/56	2=REMOVABLE 3=FIXED
10	OFF	ON	OFF	ON	0,1	0	80MB CMD 16MB CMD	823/5/56 823/1/56	0=FIXED 1=REMOVABLE
					2,3	2	80MB CMD 16MB CMD	823/5/56 823/1/56	2=FIXED 3=REMOVABLE
11	OFF	ON	OFF	OFF	0,1,2,3	0	16MB CMD/DFR	823/1/56	0=REMOVABLE
							16MB CMD/DFR	823/1/56	1=FIXED HEAD 0
							16MB CMD/DFR	823/1/56	2=FIXED HEAD 1
							16MB CMD/DFR	823/1/56	3=FIXED HEAD 2
12	OFF	OFF	ON	ON	0,1,2,3	0	16MB CMD/DFR	823/1/56	0=FIXED HEAD 0
							16MB CMD/DFR	823/1/56	1=REMOVABLE
							16MB CMD/DFR	823/1/56	2=FIXED HEAD 1
							16MB CMD/DFR	823/1/56	3=FIXED HEAD 2
13	OFF	OFF	ON	OFF	0,1,2,3	0,1,2,3	34MB 3350	561/3/56	(PRIAM)
14	OFF	OFF	OFF	ON	0,1,2,3	0,1,2,3	67MB 6650	1121/3/56	(PRIAM)
15	OFF	OFF	OFF	OFF	0,1,2,3	0,1,2,3	155MB 15450	1121/7/56	(PRIAM)

STORE REGISTER VALUES VERSION M1

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	1F80	3800	3A4D	84MB 2312
1	0,1,2 3	1F80 1F80	3800 3800	2B37 9B37	80MB SMD 300MB SMD
2	0,1,2 3	1F80 1F80	3800 3800	9B37 2B37	300MB SMD 80MB SMD
3	0,1,2 3	1F80 1F80	3800 3800	5337 9B37	160MB MMD 300MB MMD
4	0,1,2,3	1F80	3800	2B37	80MB SMD
5	0,1,2,3	1F80	3800	0B36	16MB CMD/DFR
6	0,1,2,3	1F80	3800	0B36	16MB CMD/DFR
7	0,2 1,3	1F80 1F80	3800 3800	0B36 1B36	16MB CMD/DFR 48MB CMD/DFR
8	0,2 1,3	1F80 1F80	3800 3800	1B36 0B36	48MB CMD/DFR 16MB CMD/DFR
9	0,2 1,3	1F80 1F80	3800 3800	0B36 2B36	16MB CMD/DFR 80MB CMD/DFR
10	0,2 1,3	1F80 1F80	3800 3800	2B36 0B36	80MB CMD/DFR 16MB CMD/DFR
11	0,1,2,3	1F80	3800	0B36	16MB CMD/DFR
12	0,1,2,3	1F80	3800	0B36	16MB CMD/DFR
13	0,1,2,3	1F80	3800	1A30	34MB PRIAM 3350
14	0,1,2,3	1F80	3800	1C61	67MB PRIAM 6650
15	0,1,2,3	1F80	3800	3C61	155MB PRIAM 15450

S16/26 MODEL NDRIVE CONFIGURATION TABLE
VERSION N2

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/64	(FUJITSU)
1	ON	ON	ON	OFF	0,1,2,3	0,1,2,3	160MB 9715	823/10/64	(CDC FSD I)
2	ON	ON	OFF	ON	0,1,2	0,1,2	160MB 9715	823/10/64	(CDC FSD I)
					3	3	300MB SMD	823/19/64	
3	ON	ON	OFF	OFF	0,1,2	0,1,2	160MB 9715	823/10/64	(CDC FSD I)
					3	3	340MB 9715	711/24/64	(CDC FSD IB)
4	ON	OFF	ON	ON	0,1,2	0,1,2	300MB SMD	823/19/64	
					3	3	160MB 9715	823/10/64	(CDC FSD I)
5	ON	OFF	ON	OFF	0,1,2,3	0,1,2,3	300MB SMD	823/19/64	
6	ON	OFF	OFF	ON	0,1,2	0,1,2	300MB SMD	823/19/64	
					3	3	340MB 9715	711/24/64	(CDC FSD IB)
7	ON	OFF	OFF	OFF	0,1,2	0,1,2	340MB 9715	711/24/64	(CDC FSD IB)
					3	3	160MB 9715	823/10/64	(CDC FSD I)

*When using a Fujitsu 2322-168 Mbyte drive for any of the 160 Mbyte drive types, the drive MUST be set as follows:

- Use 64 sectors/track.
- Set byte/sector count to 319.

(NOTE: This is ONE BYTE LESS than the drive chart indicates for 64 sectors).

S16/26 MODEL NDRIVE CONFIGURATION TABLE
VERSION N2

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,1,2	0,1,2	340MB 9715	711/24/64	(CDC FSD IB)
					3	3	300MB SMD	823/19/64	
9	OFF	ON	ON	OFF	0,1,2,3	0,1,2,3	340MB 9715	711/24/64	(CDC FSD IB)
10	OFF	ON	OFF	ON	0,1,2	0,1,2	160MB 9715	823/10/64	(CDC FSD I)
					3	3	500MB 9715	711/24/95	(CDC FSD II)
11	OFF	ON	OFF	OFF	0,1,2	0,1,2	300MB SMD	823/19/64	
					3	3	500MB 9715	711/24/95	(CDC FSD II)
12	OFF	OFF	ON	ON	0,1,2	0,1,2	340MB 9715	711/24/64	(CDC FSD IB)
					3	3	500MB 9715	711/24/95	(CDC FSD II)
13	OFF	OFF	ON	OFF	0,1,2	0,1,2	500MB 9715	711/24/95	(CDC FSD II)
					3	3	160MB 9715	823/10/64	(CDC FSD I)
14	OFF	OFF	OFF	ON	0,1,2	0,1,2	500MB 9715	711/24/95	(CDC FSD II)
					3	3	300MB SMD	823/19/64	
15	OFF	OFF	OFF	OFF	0	0	1/4 OF 160MB	823/10/64	CYLS 0 - 204
					1	0	1/4 OF 160MB	823/10/64	CYLS 205 - 409
					2	0	1/4 OF 160MB	823/10/64	CYLS 410 - 614
					3	0	1/4 OF 160MB	823/10/64	CYLS 615 - 819

STORE REGISTER VALUES VERSION N2

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0,1,2,3	2000	4000	532B	5335	160MB SMD
2	0,1,2 3	2000 2000	4000 4000	532B 9B2B	5335 9B35	160MB 9715-160 300MB SMD
3	0,1,2 3	2000 2000	4000 4000	532B C2BB	5335 C2C5	160MB 9715-160 340MB 9715-340
4	0,1,2 3	2000 2000	4000 4000	9B2B 532B	9B35 5335	300MB SMD 160MB 9715-160
5	0,1,2,3	2000	4000	9B2B	9B35	300MB SMD
6	0,1,2 3	2000 2000	4000 4000	9B2B C2BB	9B35 C2C5	300MB SMD 340MB 9715-340
7	0,1,2 3	2000 2000	4000 4000	C2BB 532B	C2C5 5335	340MB 9715-340 160MB 9715-160
8	0,1,2 3	2000 2000	4000 4000	C2BB 9B2B	C2C5 9B35	340MB 9715-340 300MB SMD
9	0,1,2,3	2000	4000	C2BB	C2C5	340MB 9715-340
10	0,1,2 3	2000 2F80	4000 5F00	532B C2BB	5335 C2C5	160MB 9715-160 500MB 9715-500
11	0,1,2 3	2000 2F80	4000 5F00	9B2B C2BB	9B35 C2C5	300MB SMD 500MB 9715-500
12	0,1,2 3	2000 2F80	4000 5F00	C2BB C2BB	C2C5 C2C5	340MB 9715-340 500MB 9715-500
13	0,1,2 3	2F80 2000	5F00 4000	C2BB 532B	C2C5 5335	500MB 9715-500 160MB 9715-160
14	0,1,2 3	2F80 2000	5F00 4000	C2BB 9B2B	C2C5 9B35	500MB 9715-500 300MB SMD
15	0,1,2,3	2000	4000	50C1	50CB	160MB 9715-160

S16/26 MODEL PDRIVE CONFIGURATION TABLE
VERSION P2

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/56	(FUJITSU)
1	ON	ON	ON	OFF	0,1,2,3	0,1,2,3	160MB 9715	823/10/56	(CDC FSD I)
2	ON	ON	OFF	ON	0,1,2	0,1,2	160MB 9715	823/10/56	(CDC FSD I)
					3	3	300MB SMD	823/19/56	
3	ON	ON	OFF	OFF	0,1,2	0,1,2	160MB 9715	823/10/56	(CDC FSD I)
					3	3	340MB 9715	711/24/56	(CDC FSD IB)
4	ON	OFF	ON	ON	0,1,2	0,1,2	300MB SMD	823/19/56	
					3	3	160MB 9715	823/10/56	(CDC FSD I)
5	ON	OFF	ON	OFF	0,1,2,3	0,1,2,3	300MB SMD	823/19/56	
6	ON	OFF	OFF	ON	0,1,2	0,1,2	300MB SMD	823/19/56	
					3	3	340MB 9715	711/24/56	(CDC FSD IB)
7	ON	OFF	OFF	OFF	0,1,2	0,1,2	340MB 9715	711/24/56	(CDC FSD IB)
					3	3	160MB 9715	823/10/56	(CDC FSD I)

S16/26 MODEL PDRIVE CONFIGURATION TABLE
VERSION P2

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,1,2	0,1,2	340MB 9715	711/24/56	(CDC FSD IB)
					3	3	300MB SMD	823/19/56	
9	OFF	ON	ON	OFF	0,1,2,3	0,1,2,3	340MB 9715	711/24/56	(CDC FSD IB)
10	OFF	ON	OFF	ON	0,1,2	0,1,2	160MB 9715	823/10/56	(CDC FSD I)
					3	3	500MB 9715	711/24/86	(CDC FSD II)
11	OFF	ON	OFF	OFF	0,1,2	0,1,2	300MB SMD	823/19/56	
					3	3	500MB 9715	711/24/86	(CDC FSD II)
12	OFF	OFF	ON	ON	0,1,2	0,1,2	340MB 9715	711/24/56	(CDC FSD IB)
					3	3	500MB 9715	711/24/86	(CDC FSD II)
13	OFF	OFF	ON	OFF	0,1,2	0,1,2	500MB 9715	711/24/86	(CDC FSD II)
					3	3	160MB 9715	823/10/56	(CDC FSD I)
14	OFF	OFF	OFF	ON	0,1,2	0,1,2	500MB 9715	711/24/86	(CDC FSD II)
					3	3	300MB SMD	823/19/56	
15	OFF	OFF	OFF	OFF	0	0	1/4 OF 160MB	823/10/56	CYLS 0 - 204
					1	0	1/4 OF 160MB	823/10/56	CYLS 205 - 409
					2	0	1/4 OF 160MB	823/10/56	CYLS 410 - 614
					3	0	1/4 OF 160MB	823/10/56	CYLS 615 - 819

STORE REGISTER VALUES VERSION P2

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	1F80	3800	3A4D	84MB 2312
1	0,1,2,3	1F80	3800	5337	160MB SMD
2	0,1,2 3	1F80 1F80	3800 3800	5337 9B37	160MB 9715-160 300MB SMD
3	0,1,2 3	1F80 1F80	3800 3800	5337 C2C7	160MB 9715-160 340MB 9715-340
4	0,1,2 3	1F80 1F80	3800 3800	9B37 5337	300MB SMD 160MB 9715-160
5	0,1,2,3	1F80	3800	9B37	300MB SMD
6	0,1,2 3	1F80 1F80	3800 3800	9B37 C2C7	300MB SMD 340MB 9715-340
7	0,1,2 3	1F80 1F80	3800 3800	C2C7 5337	340MB 9715-340 160MB 9715-160
8	0,1,2 3	1F80 1F80	3800 3800	C2C7 9B37	340MB 9715-340 300MB SMD
9	0,1,2,3	1F80	3800	C2C7	340MB 9715-340
10	0,1,2 3	1F80 3060	3800 5600	5337 C2C7	160MB 9715-160 500MB 9715-500
11	0,1,2 3	1F80 3060	3800 5600	9B37 C2C7	300MB SMD 500MB 9715-500
12	0,1,2 3	1F80 3060	3800 5800	C2C7 C2C7	340MB 9715-340 500MB 9715-500
13	0,1,2 3	3060 1F80	5600 3800	C2C7 5337	500MB 9715-500 160MB 9715-160
14	0,1,2 3	3060 1F80	5600 3800	C2C7 9B37	500MB 9715-500 300MB SMD
15	0,1,2,3	1F80	3800	50CD	160MB 9715-160

S16/26 MODEL TDRIVE CONFIGURATION TABLE
VERSION T1

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
0	ON	ON	ON	ON	0,1,2,3	0,1,2,3	84MB 2312	589/7/64	(FUJITSU)
1	ON	ON	ON	OFF	0,1,2	0,1,2	80MB SMD	823/5/64	
					3	3	300MB SMD	823/19/64	
2	ON	ON	OFF	ON	0,1,2	0,1,2	300MB SMD	823/19/64	
					3	3	80MB SMD	823/5/64	
3	ON	ON	OFF	OFF	0,1,2	0,1,2	80MB SMD	815/5/61	
					3	3	300MB SMD	815/19/61	
4	ON	OFF	ON	ON	0,1,2	0,1,2	300MB SMD	815/19/61	
					3	3	80MB SMD	815/5/61	
5	ON	OFF	ON	OFF	0,1,2,3	0,1,2,3	160MB STD	823/10/64*	
6	ON	OFF	OFF	ON	0,1	0	160MB STD	823/10/64	0=HEADS 0-4 1=HEADS 5-9
					2,3	2	160MB STD	823/10/64	0=HEADS 0-4 1=HEADS 5-9
7	ON	OFF	OFF	OFF	0,1	0	160MB STD	815/10/61	0=HEADS 0-4 1=HEADS 5-9
					2,3	2	160MB STD	815/10/61	0=HEADS 0-4 1=HEADS 5-9

*When using a Fujitsu 2322-168 Mbyte drive for any of the 160 Mbyte drive types, the drive MUST be set as follows.

-Use 64 sectors/track.

-Set byte/sector count to 319.

(NOTE: This is ONE BYTE LESS than the drive chart indicates for 64 sectors).

S16/26 MODEL TDRIVE CONFIGURATION TABLE
VERSION T1

	4	3	2	1	LOGICAL UNIT #	PHYSICAL UNIT #	DRIVE	CYL/HD/SEC	COMMENTS
8	OFF	ON	ON	ON	0,1	0	160MB STD	815/10/61	0=HEADS 0-4 1=HEADS 5-9
					2,3	2,3	80MB SMD	815/5/61	
9	OFF	ON	ON	OFF	0,3	0,3	80MB SMD	815/5/61	
					1,2	1	160MB STD	815/10/61	1=HEADS 0-4 2=HEADS 5-9
10	OFF	ON	OFF	ON	0,1	0	675MB STD	815/40/61	
					2,3	2,3	300MB SMD	815/19/61	
11	OFF	ON	OFF	OFF	0,3	0,3	300MB SMD	823/19/56	
					1,2	1	675MB CDC	843/40/61	1=HEADS 0-18 2=HEADS 19-37
12	OFF	OFF	ON	ON	0,1	0	474MB 2351	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2	474MB 2351	842/20/88	2=HEADS 0-9 3=HEADS 10-19
13	OFF	OFF	ON	OFF	0,1,2,3	0,1,2,3	330MB C330	1024/16/64	
14	OFF	OFF	OFF	ON	0,1,2,3	0,1,2,3	160MB STD	1645/5/64	
15	OFF	OFF	OFF	OFF	0,1	0	474MB 2351	842/20/88	0=HEADS 0-9 1=HEADS 10-19
					2,3	2,3	300MB SMD	823/19/64	

STORE REGISTER VALUES VERSION T1

Two different values are given for WORD 2. The first value assumes the alternate track feature is enabled. The second value is returned if the alternate track feature is disabled.

<u>SETTING</u>	<u>LOGICAL DRIVE #</u>	<u>WORD 0</u>	<u>WORD 1</u>	<u>WORD 2</u>	<u>WORD 2</u>	<u>DRIVE</u>
0	0,1,2,3	2000	4000	3A41	3A4B	84MB 2312
1	0,1,2 3	2000 2000	4000 4000	2B2B 9B2B	2B35 9B35	80MB SMD 300MB SMD
2	0,1,2 3	2000 2000	4000 4000	9B2B 2B2B	9B35 2B35	300MB SMD 80MB SMD
3	0,1,2 3	1E80 1E80	3D00 3D00	2B23 9B23	2B23 9B23	80MB SMD 300MB SMD
4	0,1,2 3	1E80 1E80	3D00 3D00	9B23 2B23	9B23 2B23	300MB SMD 80MB SMD
5	0,1,2,3	2000	4000	532B	5335	160MB SMD
6	0,1,2,3	2000	4000	2B2B	2B35	80MB SMD
7	0,1,2,3	1E80	3D00	2B23	2B23	80MB SMD
8	0,1,2,3	1E80	3D00	2B23	2B23	80MB SMD
9	0,1,2,3	1E80	3D00	2B23	2B23	80MB SMD
10	0,1,2,3	1E80	3D00	9B23	9B23	300MB SMD
11	0,1,2,3	1E80	3D00	9B23	9B23	300MB SMD
12	0,1,2,3	2C00	5800	533E	5348	474MB 2351
13	0,1,2,3	2000	4000	83F4	83FE	330MB C330
14	0,1,2,3	2000	4000	2E61	2E6B	160MB SMD
15	0,1 2,3	2C00 2000	5800 4000	533E 9B2B	5348 9B35	474MB 2351 300MB SMD

2.4 CABLE CONNECTIONS

Disk Drive

Prior to connecting the interface cables, ensure that the drive unit number and sectors per track settings are correct. Also, the drive must be set for hard sectoring (a fixed number of sectors/track). The SPECTRA 16/26/36 does not detect soft sectoring (using address marks).

To connect the interface cables to the controller board, connect the 60 conductor 'A' cable connector to the J1 header on the controller PCB. Ensure that pin 1 of the cable connector mates with pin 1 of the PCB header; pin 1 is designated by a small arrowhead and the brown/tan twisted pair.

Connect the 26 conductor 'B' cable connector to the J2 header on the controller. Again, ensure that pin 1 of the cable connector mates with pin 1 of the PCB header; pin 1 is designated by a small arrowhead and cable stripe.

To connect the interface cables to the disk drive, route all cables neatly out of the CPU chassis. Connect the 60 conductor 'A' cable to the first disk drive, and if more than one drive is attached, daisy chain the 'A' cable between units. Install a terminator on the last drive in the chain. Then connect one 26 conductor 'B' cable to each drive. It is recommended that a ground braid be attached between the CPU chassis and each disk drive chassis.

Tape Drive

Consult the tape drive manual for the list of interface signals for each connector. Pin 2 of one connector has a signal called "FBY" or "IFBY". This connector receives the cable coming from J6 on the controller. The other connector on the tape drive connects to J7 on the controller. The 50 conductor tape cables should be connected to the J6 and J7 headers. Ensure that pin 1 of each is mated.

2.5 INSTALLATION into CPU

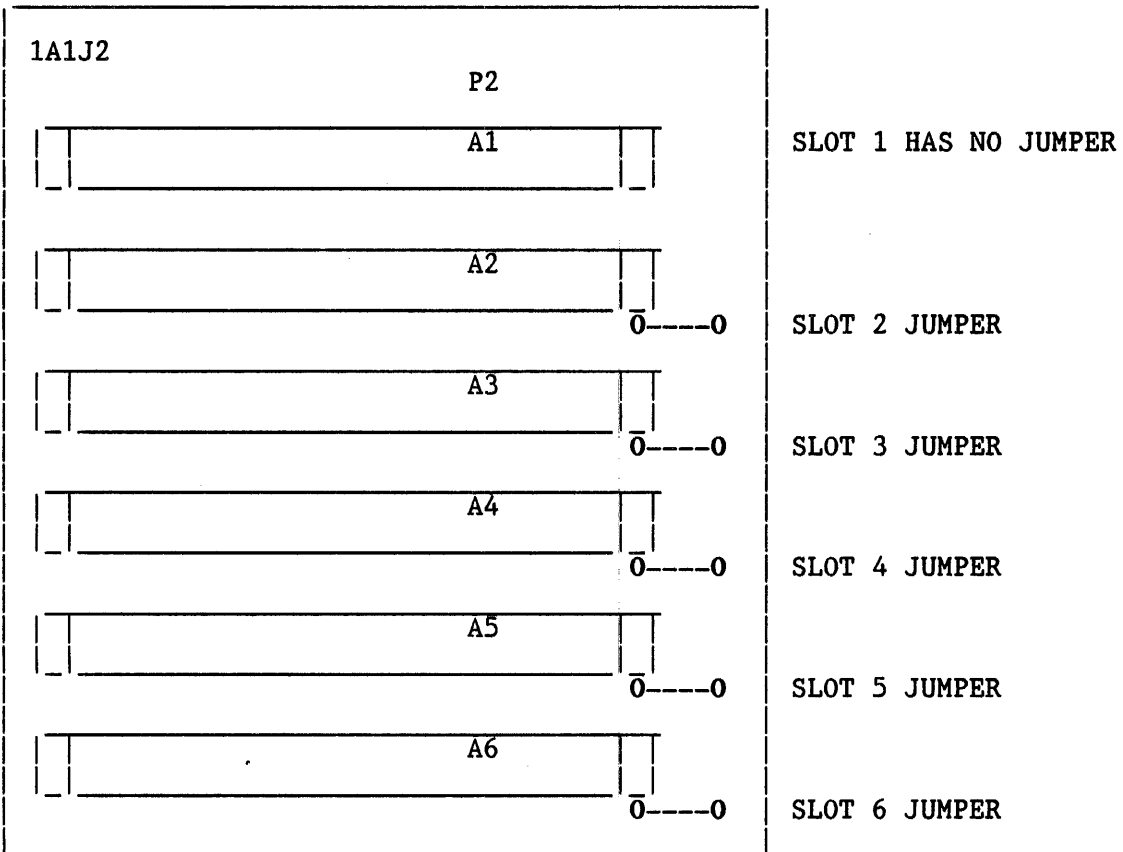
The SPECTRA 16/26/36 may be installed in any peripheral slot in the CPU or expansion chassis. Ensure that power is off before inserting or removing the board to avoid any possible damage. DC voltage should be measured on the PCB and adjusted, if necessary, to 5 volts $\pm 5\%$.

2.5.1 PREPARING a CHASSIS SLOT

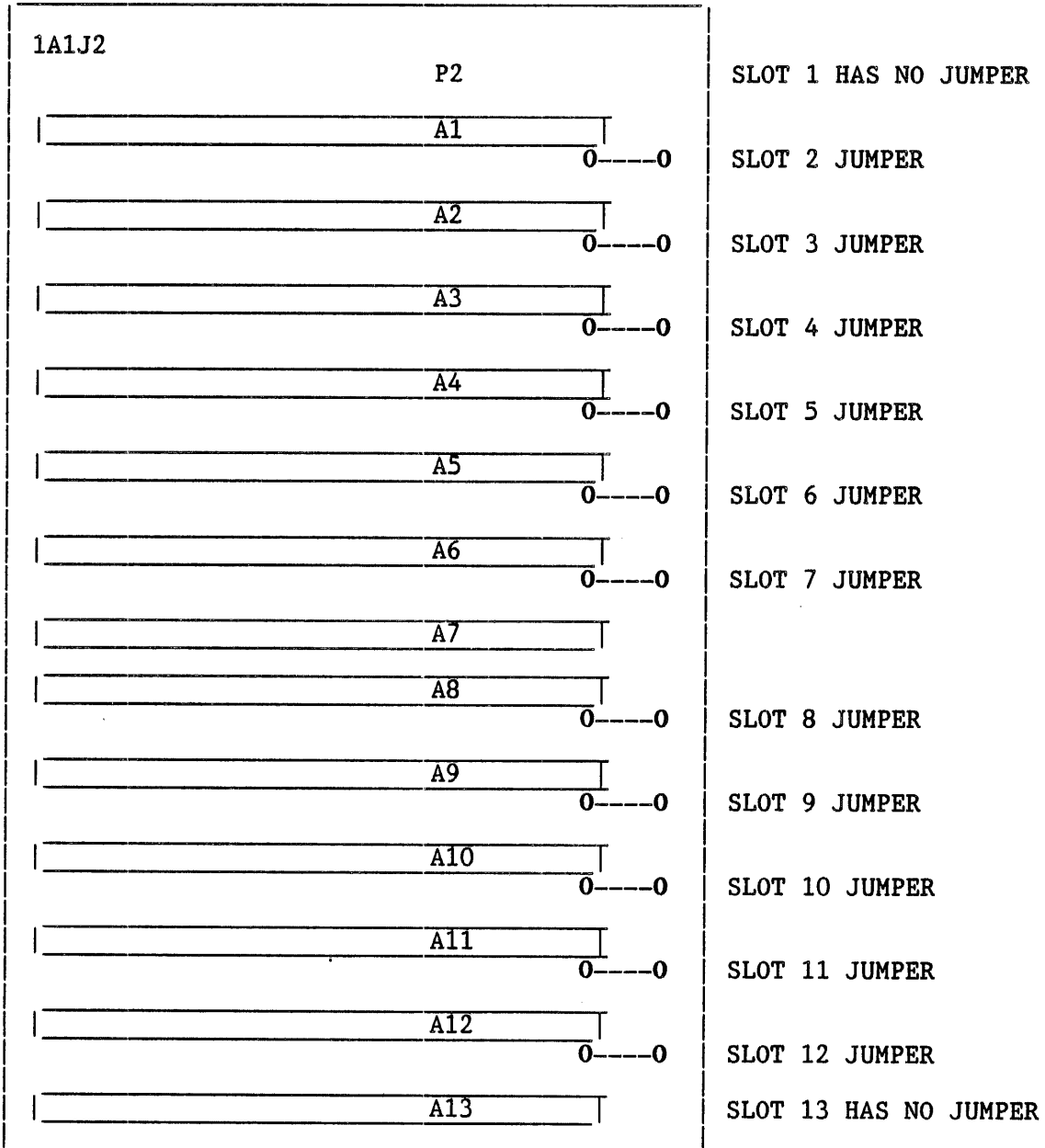
Before the SPECTRA 16/26/36 can be installed, the TILINE Access Granted (TLAG) jumper must be removed. The modifications to the various chassis versions follow. For further information, see the Model 990/10 Computer System Hardware Reference Manual. Do not attempt any modifications with AC power connected.

Current Production (6-slot)

1. Remove any circuit boards necessary for access to TLAG plug.
2. Remove TLAG plug for selected location.
3. Replace circuit boards.



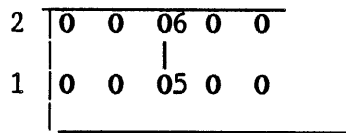
Current Production (13-slot)



Early Production (6 and 13-slot)

1. Remove left access cover.
2. Remove power supply and RF shield.
3. Cut trace or wire between P2-5 and P2-6 (TLAG).
4. Re-install power supply, RF shield, and access cover.

The following diagram is the rear view of the 990 Motherboard (power supply side).

**Current Production (17-Slot)**

1. Remove the rear chassis cover.
2. The TLAG switches are located below the power supply.
3. If a switch is on, it indicates the TLAG is jumpered across slot (P2-6 to P2-5). If a switch is off, it indicates that the TLAG signal is not jumpered.

<u>SWITCH</u>	<u>SLOT</u>	<u>SWITCH</u>	<u>SLOT</u>
2-1	2	1-1	10
2-2	3	1-2	11
2-3	4	1-3	12
2-4	5	1-4	13
2-5	6	1-5	14
2-6	7	1-6	15
2-7	8	1-7	16
2-8	9	1-8	N/C

Interrupt Connections

The SPECTRA 16/26/36 has the disk interrupt available at P2-66 and the tape interrupt available at P1-66. The 990 CPU comes with standard interrupt settings. Ensure that P1-66 and P2-66 are not connected together for the slot containing the SPECTRA 16/26/36. For further information concerning interrupt changes, consult the TI System Hardware Reference Manual.

Chapter Three

Theory of Operation

3.1 THEORY OF OPERATION

The SPECTRA 16/26/36 multifunction disk and tape controller is a dual microprocessor design employing bit slice microprogrammable technology. The two microprocessors perform independent functions to simultaneously control the TILINE interface. The microprocessor controlling the TILINE interface is referred to as the CPU Microprocessor (CM), and the microprocessor controlling SMD interface is referred to as the Disk Microprocessor (DM).

The CPU Microprocessor is responsible for command decoding, command initiation, command termination, data transfer operations, final status, and interrupt request generation. The CPU microprocessor also allocates time to the disk and tape units during concurrent data transfer operations.

The Disk Microprocessor controls the SMD interface, selects the disk drive, and generates tag and bus information to the drive. It controls read/write operations, serialization/deserialization, sector format, CRC, and ECC. Additionally, the Disk Microprocessor accesses the sector data buffer during read and write operations to transfer bytes of data between the buffer and serializer/deserializer. It also reads drive status from the SMD interface and stores it into the appropriate status register.

The two microprocessors communicate with each other through the first 512 bytes of the 2K byte RAM buffer. The CM loads the disk registers as addressed during I/O write operations into the space designated in the RAM buffer. Once a command is given with the GO flip-flop set, the CM sets a flag in the buffer to inform the DM that there is a command to perform. When the DM accepts the command, it resets the flag. The DM sets the ATTENTION flip-flop when it has completed a command and updated the status. The CM waits for ATTENTION before completing the termination and setting DONE. Whenever the SPECTRA 16/26/36 does not have a command active, both microprocessors go into an idle loop. The CM waits for a new command while the DM polls the two disk drive ports to update and maintain drive status.

The upper 1536 words of the RAM data buffer are shared between the two microprocessors to provide up to 3 sectors of data buffering during read/write operations. During write operations, a sector buffer full flag is set to inform the DM once a sector of data has been transferred to the buffer from the TILINE via the CM. Additionally, a 64 byte FIFO is used to buffer data between the formatted tape drive and the CPU.

3.1.1 THE CPU MICROPROCESSOR

The CPU Microprocessor (CM) is a bit slice design using four 2901 processors and two major busses, CSRC and CDEST. The CSRC BUS is a 16-bit wide data path providing the four 2901 bit slice processors a source for their "D" inputs. Data on the CSRC BUS may be selected from TILINE data, DIP switches, tape input data, the RAM data buffer, and constants from the control store literal field. The CDEST BUS is a 16-bit wide data path used for 2901 "Y" output destination. A variety of destinations may be selected for the CDEST such as TILINE data, TILINE address, tape data, RAM data buffer address, and RAM data buffer data.

The CPU microprocessor also consists of three 2911 sequencers. The sequencers address the control store from its program counter, perform jumps, conditional jumps, subroutine jumps, and subroutine returns. Up to four levels of subroutines may be nested in the sequencer's stack. When Interrupt Enable (IE) is set, interrupts occur on memory error or TILINE address comparison.

The instruction width of the CPU microprocessor is 48 bits. Six 1Kx8 PROMs are used to form a 1Kx48 control store containing the firmware for the CM. The instruction word is defined below.

CPU MICROPROCESSOR INSTRUCTION WORD BIT DEFINITIONS

BIT	NAME	FUNCTION
47-45	NA NEXT ADDRESS	These bits provide the next address control inputs (decoded by a 74S288 PROM) that define the type of jump to be performed.
44	TINT TILINE INTERR	This bit enables TILINE address comparison interrupt.
43	MEM ERR MEMORY ERROR	This bit enables Memory Error interrupts.
42-40	CSRC ADD 0-2 CPU SOURCE ADDRESS	These bits define one of eight sources of input to the 2901 processors on the CSRC BUS.
39-37	CDEST ADD 0-2 CPU DESTINATION ADDRESS	These bits define one of eight destinations to route output information from the 2901 processors on the CDEST BUS.
36	CCN CPU CARRY-IN	This bit enables carry-in control.

CPU MICROPROCESSOR
INSTRUCTION WORD BIT DEFINITIONS

BIT	NAME	FUNCTION
35-27	CI CPU INSTRUCTION	These bits provide the instruction input to the 2901 processors.
26-23	CRA CPU REGISTER ADDRESS	These bits supply the 2901 processors' A input address to select one of 16 registers in the 2901 processors.
22	FLGINS FLAG INSTRUCTION	For instructions using the flag field, the 2901's B input address will be the same as the A input address. For instructions not using the flag field, flag address bits 5-2 will supply the B input address.
21-16	FLGADD FLAG ADDRESS	For instructions using the flag field, these bits are decoded to select one of several flags. Depending on the address, flags may either be latched or pulsed.
15-0	CPD CPU PROM DATA	These bits supply a 16-bit constant on the CSRC BUS for instructions using a constant. For jump instructions, bits 15-5 supply the processors with a next address. For conditional jump instructions, bits 4-0 are decoded to select a branch condition to be tested.

3.1.2 THE DISK MICROPROCESSOR

The Disk Microprocessor (DM) is a bit slice design using two 2901 processors. The two processors form an 8-bit data path to perform arithmetic, logical, and shift operations. The two major busses used by the DM are DSRC and DDEST. The DSRC bus provides an 8-bit wide data path used for the 2901 processor's input source on their "D" inputs. The firmware may select several input sources such as serializer/deserializer data, the drive configuration PROM, drive status, the data buffer, and DIP switches. The DDEST bus provides an 8-bit wide data path used for 2901 "Y" output destination. Selectable destinations include the data buffer address, data buffer data, branch condition input, serializer/deserializer data, the serializer/deserializer control register, and the SMD interface control registers.

The DM also uses three 2911 sequencers, as used in the CM. The sequencers address the control store from its program counter, perform jumps, conditional jumps, subroutine jumps, and subroutine returns. Interrupt capability is not provided by the DM's sequencers.

The instruction width of the Disk Microprocessor is 32 bits. Four 1Kx8 PROMs are used to form a 1Kx32 control store which contains the firmware. The DM instruction word is described below.

DISK MICROPROCESSOR INSTRUCTION WORD BIT DEFINITIONS

BIT	NAME	FUNCTION
31-30	DISK PROM DATA	These bits define the type of jump to be performed.
29-27	DSRC DISK SOURCE	These bits are decoded to determine one of 8 sources of information to be placed on the DSRC bus.
26-23	DDEST DISK DESTINATION	These bits are decoded to determine which register or control function is strobed with information on the DDEST bus.
22	DISK CARRY-IN	This bit enables carry-in control.
21-13	DISK INSTRUCTION	These bits provide the instruction input to the 2901 processors.
12	DISK FLAG ENABLE	This bit enables pulsed or latched flags to be generated from data on DPIPE 31-24.
11-0	DISK PIPELINE	These bits are stored in two LS273 registers to provide address input to the 2911 sequencers, jump target address, flag selection for instructions using the flag enable, A and B input addresses for the 2901 processors, and a constant value for instructions using a constant.

3.1.3 DISK INTERFACE

The SMD disk interface is controlled by the Disk Microprocessor. The firmware transmits information on the SMD bus and tag lines by loading the 74LS273 registers. MC3453 quad line drivers drive the SMD interface lines, and MC3450 quad line receivers are used to receive signals on the SMD interface. The DM controls selection of the logical disk drive, interrupt status from the drive, cylinder/head addressing, and READ/WRITE operations.

The serializer/deserializer uses two 74S299 registers to form a 16-bit shift register to convert data from parallel to serial during Write operations, and from serial to parallel during Read operations. During Write operations, parallel data is transferred from the data buffer and loaded 8 bits at a time into the 74S299 shift registers. During Read operations, data is transferred from the S/D shift register into two 74LS374 registers and then into the data buffer. The data buffer is comprised of four 2149 RAMs and two 74S374 registers.

The DM firmware is synchronized to the SMD interface by a bit counter which sets a word available flip-flop (WRDAV) each time the counter overflows. A control register is also clocked by the counter overflow to synchronize firmware control information previously stored in a 74LS273 register. This register synchronizes switching of ECC logic enable, ECC reset, and ECC clock enable. These controls are pre-loaded by the firmware into a holding register in the previous word time and are enabled at the next word available time.

The Error Correction Code (ECC) polynomial is implemented with four 74LS164 registers hooked up as a barrel shifter with a parity tree providing the feedback for each term of the polynomial. The polynomial used in this design is:

$$X^{32} + X^{30} + X^{29} + X^{27} + X^{17} + X^{15} + X^5 + X^3 + 1$$

The ECC feedback is enabled by the CWE signal under firmware control. The clock driving the ECC logic is also enabled by firmware and may be taken from read clock, servo clock, the half frequency controller clock, or a firmware generated ECC CLK. These same four sources generate the bit clock to drive the serializer/deserializer.

3.1.4 TAPE INTERFACE

The Pertec compatible formatted tape interface is controlled by the CPU microprocessor via the CDEST bus. This 16-bit bus is clocked into two 74LS273 octal latches which drive tape control lines and initiate the micro sequencer, which consists of an octal latch and a 512 x 8 bit PROM (74S472). The micro sequencer issues clocks and other internal control signals to the magnetic tape control circuitry.

The input and output data flows through two 67402 FIFOs which create a 64 byte buffer. A 74S280 generates the Write Parity (WP) bit during Write operations. Write data is clocked off of the CDEST bus through 74LS374 latches into the FIFO buffers. Read data is clocked out of the FIFO buffers, through latches, onto the CSRC bus, and back to the CPU microprocessor.

3.2 DISK REGISTER DEFINITIONS

The control and status words on the SPECTRA 16/26 are used for both operating the controller and reporting disk system status. The CPU can write Control Words into controller registers to initiate operation, and can read Status Words in these registers to determine disk status upon completion of an operation. Some bits in these registers are used for disk operation control, some for status reporting, and some for both control and status. A summary of the Control and Status words is shown below.

<u>CONTROL WORD</u>	<u>CPU BYTE ADDRESS</u>	<u>TILINE WORD ADDRESS</u>
0	F800	FFC00
1	F802	FFC01
2	F804	FFC02
3	F806	FFC03
4	F808	FFC04
5	F80A	FFC05
6	F80C	FFC06
7	F80E	FFC07

CONTROL WORD 0

DISK STATUS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	NR	WP	UNS	EC	SKI	OSA	0	ATA	ATA	ATA	ATA	AIM	AIM	AIM	AIM

CONTROL WORD 1

FORMAT AND COMMAND

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EXA	EXB	SE	SL	TIH	COM	COM	COM	OS	OSF	HA	HA	HA	HA	HA	HA

CONTROL WORD 2

SECTOR

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SPR	SPR	SPR	SPR	SPR	SPR	SPR	SPR	SSA	SSA	SSA	SSA	SSA	SSA	SSA	SSA

CONTROL WORD 3

CYLINDER ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA

CONTROL WORD 4

WORD COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC

CONTROL WORD 5

MEMORY ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA

CONTROL WORD 6

SELECT AND MEMORY ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	DS	DS	DS	DS	0	0	0	MA	MA	MA	MA	MA

CONTROL WORD 7

CONTROLLER STATUS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	CP	ERR	INT	LO	RT	ECC	AC	ME	DE	TO	IE	RE	CT	SE	UE

CONTROL WORD 0 DISK STATUS

This word contains disk status codes for the selected drive. It also contains attention bits and attention mask bits for generating interrupts.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	NR	WP	UNS	EC	SKI	OSA	0	ATA	ATA	ATA	ATA	AIM	AIM	AIM	AIM

BIT	NAME	FUNCTION
0	OFL Offline	Set if the drive is not powered on, not up to speed, does not have a cartridge or pack loaded, or is in an unsafe condition.
1	NR Not Ready	When set, indicates that the drive is off line or executing a RESTORE command.
2	WP Write Protect	When set, indicates that the drive is write protected.
3	UNS Unsafe	When set, this bit indicates that the drive is in an unsafe condition preventing normal disk operation. Cleared by issuing a RESTORE or a STORE REGISTERS command (if the unsafe condition no longer exists).
4	EC End of Cylinder	This bit is always zero.
5	SKI Seek Incomplete	Set when the drive fails to complete a seek operation and reports seek incomplete status. A restore operation is required to recover.
6	OSA Offset Active	Not used. Always zero.
7	---	Not used. Always zero.
8-11	ATA Attention	Attention bits for drives 0-3.
12-15	AIM Attention Interrupt Mask	If an Attention Mask bit and its corresponding attention bit are both set, an interrupt to the 990 is generated. These bits are used with overlap seek operation on multiple non-mapped disk drives.

CONTROL WORD 1 FORMAT AND COMMAND

This word contains command codes, head address, and several control bits used during certain data recovery operations.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EXA	EXB	SE	SL	TIH	COM	COM	COM	OS	OSF	HA	HA	HA	HA	HA	HA

BIT	NAME	FUNCTION
0-1	EXT A&B Extended Commands A&B	These bits work in conjunction with the command bits 7-5 so that they are interpreted as ten additional commands.
2	SE Strobe Early	When set, this bit enables a strobe early condition.
3	SL Strobe Late	When set, this bit enables a strobe late condition.
4	TIH Transfer Inhibit	When set, this bit inhibits the transfer of data to the TILINE interface during read operations. Data is checked for ECC errors with no transfer to main memory.
5-7	COM Command	These bits represent normal commands. The commands are shown in table 3-1.
8	OS Head Offset	This bit is used in conjunction with bit 9 to offset the heads forward or reverse from nominal during reads.
9	OSF Head Offset	This bit is set to 1 for offset forward, and to 0 for offset reverse.
10-15	HA Head Address	These bits select the Read/Write heads as follows: 15 = H ₁ 14 = H ₂ 13 = H ₄ 12 = H ₈ 11 = H ₁₆ 10 = H ₃₂

TABLE 3-1 COMMAND CODES

BIT 0	BIT 1	BIT 5	BIT 6	BIT 7	COMMAND
0	0	0	0	0	STORE REGISTERS
0	0	0	0	1	WRITE FORMAT
0	0	0	1	0	READ DATA
0	0	0	1	1	WRITE DATA
0	0	1	0	0	READ UNFORMATTED (3)
0	0	1	0	1	WRITE UNFORMATTED
0	0	1	1	0	SEEK (1)
0	0	1	1	1	RESTORE
1	0	1	0	0	READ UNFORMATTED
1	0	1	1	1	SELF-TEST (2)
1	1	0	0	1	ABSOLUTE WRITE (5)
0	1	0	0	1	RELOCATE (5)
1	0	0	0	1	WRITE FORMAT FLAGGED(4)

- NOTES:
- 1) Seek commands are ignored for mapped drives.
 - 2) SPECTRA 16/26 microdiagnostics are not the same as the CD1400 self-tests. See section 4.3.
 - 3) Does not actually read from disk. See section 3.2.2. Reads formatted data for Model M only.
 - 4) To flag bad tracks, this command has been re-defined for use with the SPECTRA 16/26 (revision A firmware).
 - 5) Supported by revision B firmware only.

CONTROL WORD 2 SECTOR

This word contains bits which select the starting sector address and determines the number of sectors per record on the disk.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SPR	SPR	SPR	SPR	SPR	SPR	SPR	SPR	SSA	SSA	SSA	SSA	SSA	SSA	SSA	SSA

BIT	NAME	FUNCTION
0-7	SPR Sectors Per Record	These bits are ignored by the controller.
8-15	SSA Starting Sector Address	These bits select the starting sector address for all Read and Write operations (except WRITE FORMAT which does not require a starting sector address).

CONTROL WORD 3 CYLINDER

This word contains the cylinder address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA

BIT	NAME	FUNCTION
0-15	CA Cylinder Address	These bits select the cylinder address. Bit 15 is the least significant cylinder weight, ascending from right to left.

CONTROL WORD 4 WORD COUNT

This word specifies the number of bytes to be transferred between the disk and CPU memory.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC	TBC

BIT	NAME	FUNCTION
0-15	TBC Transfer Byte Count	These bits specify the number of bytes to be transferred. The byte count must be an even number. Up to 64K bytes may be transferred.

CONTROL WORD 5 LSB MEMORY ADDRESS

This word contains the 15 least significant bits of the 20-bit TILINE memory address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA	MA

BIT	NAME	FUNCTION
0-15	MA Memory Address	Bits 14-0 contain the 15 least significant bits of the 20-bit TILINE starting memory address. Bit 15 is always zero. The 5 most significant bits are in word 6

CONTROL WORD 6 SELECT AND MSB MEMORY ADDRESS

This word contains drive select codes and the 5 most significant bits of the 20-bit TILINE memory address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	DS0	DS1	DS2	DS3	0	0	0	MA	MA	MA	MA	MA

BIT	NAME	FUNCTION
0-3	----	Not used. Always zero.
7-4	DS 3-0 Drive Select	These bits contain drive select codes. They should be set one at a time.
8-10	SPARE	Not used. Always zero.
11-15	MA Memory Address	Bits 15-11 contain the 5 most significant bits of the 20-bit TILINE starting memory address.

CONTROL WORD 7 CONTROLLER STATUS

This word contains controller status codes, the Interrupt Enable (IE) bit, and the idle/busy bit.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	CP	ERR	IE	LO	RT	ECC	AC	ME	DE	TO	IDE	RE	CTO	SE	UE

BIT	NAME	FUNCTION
0	IDL Idle	When set, this bit indicates that the controller is not busy and ready to accept a new command.
1	CP Complete	Set when the controller completes a command without error.
2	ERR Error	Set if an error is detected. Bits 15-7 provide the detailed error indicators.
3	IE Interrupt Enable	This bit must be set to enable the controller to generate an interrupt on completion of a command. If IE is set while the controller is idle and the Complete or Error bit is set, an interrupt is generated immediately. Attention interrupts in word 0 are independent of the Interrupt Enable bit.
4	LO Lock Out	This bit is set when Control Word 7 is read.
5	RE Retry	Set when the controller encounters a data error causing a re-read operation to be performed.
6	ECC Corrected	Set when the controller corrects data within its buffer during a Read operation.
7	AC Abnormal Condition	Set if a disk operation is terminated due to an I/O reset, TILINE power fail warning, TILINE power reset, or if a WRITE FORMAT or WRITE UNFORMATTED command is issued with the Format Enable switch disabled.
8	ME Memory Error	Set if a TILINE memory error is detected during a disk Write operation. Any data transfer operation is terminated upon detecting a Memory Error.

CONTROL WORD 7 CONTROLLER STATUS [continued]

BIT	NAME	FUNCTION
9	DE Data Error	Set if an uncorrectable ECC error is detected during a Read operation.
10	TO Time-Out	Set if the controller's 50 microsecond timer expires before any TILINE cycle has completed. May be caused by attempting to access non-existent memory.
11	IDE ID Error	Set if an ID word non-comparison occurs during ID verification of ID words 1, 2, or 3 executing a READ DATA or WRITE DATA command.
12	RE Rate Error	Set if the TILINE is unable to keep up with the disk. This error cannot occur due to 3 sector buffering.
13	CTO Command Time Out	Set if the controller fails to complete an operation before the command timer expires.
14	SE Search Error	Set if the controller fails to detect a sync character within a physical sector during a Read operation.
15	UE Unit Error	Set if an operation is terminated due to a disk drive error.

The following table shows how a combination of bits 15 to 13 (word 7) is used to flag errors more specifically after a FORMAT command.

<u>BIT 13</u>	<u>BIT 14</u>	<u>BIT 15</u>	
0	1	0	SECTOR/INDEX SEARCH TIMEOUT
0	1	1	SECTOR COUNT ERROR
1	0	1	LOSS OF SERVO CLOCK

3.2.1 PROGRAMMING THE CONTROLLER

The SPECTRA 16/26 controller may be programmed using the eight control and status words previously described. Each control word must have the appropriate bits set or reset, depending on the desired operation. The control words must then be transmitted to the controller so that the operation may be executed. An operation is immediately executed when the controller receives Control Word 7 with bit 0 reset; therefore, Control Word 7 must be transmitted last.

Transmitting a new set of Control Words to the controller destroys the status words from the previous operation, except for the disk status bits (0-11) of Word 0. The disk status bits are set by the disk drive and cannot be modified by overwriting with a new Control Word. If overwriting is attempted, the controller does not acknowledge the new settings of the disk status bits.

Before issuing a command to the controller, bit 0 in Word 7 should be checked to verify that the controller is idle and ready to accept the command. The controller becomes busy only when it has been given a command. If bit 0 in Word 7 is zero (busy) when attempting to read status, bits 1 through 15 of this word become meaningless. If a command is issued to the controller after an operation has already been initiated, the attempt seems to complete normally, but the controller ignores the command.

3.2.2 NORMAL COMMAND DESCRIPTIONS

STORE REGISTERS COMMAND

The STORE REGISTERS command allows the operating system software to determine critical disk parameters, such as words per track and cylinders available per drive unit. This command causes the controller to send one, two, or three words to the 990 memory from the disk system, starting at the memory address specified in Control Words 5 and 6, and specified by the word count in Control Word 4. The three words contain the following information:

- WORD 0: Word 0 is the total number of unformatted words that can be recorded on a disk track. For the SPECTRA 16/26 controller, there is a fixed format as indicated by the zero value in the bytes of overhead per record parameter. The word zero value defaults to formatted words per track.
- WORD 1: Bits 0-7 of word 1 specify the number of sectors per track, and bits 8-15 specify the number of bytes of overhead per sector.
- WORD 2: Bits 0-4 of word 2 specify the number of tracks per cylinder, and bits 5-15 specify the number of cylinders per drive.

WRITE FORMAT COMMANDRevision A Firmware

The WRITE FORMAT command formats a new disk or reformats a disk already in service. One complete track is formatted per command. After receiving all command words, the controller verifies no disk status errors (offline, not ready, unsafe, write protect, offset active, or seek incomplete), seeks to the specified cylinder, and sets the specified head address. A fill word is fetched from a specified TILINE memory location. The controller assembles the ID words from its internal registers and counters and records the word(s) on the disk as header at the specified disk track address. The controller then fills the entire data field following the ID words by repeating the fill word fetched from TILINE memory. The ECC is then appended to the data field. Each sector on the track is formatted in this manner with ID words, data, ECC, and required gaps.

Revision B Firmware

If the alternate track switch is disabled, this command is performed as an ABSOLUTE WRITE FORMAT command. If the switch is enabled, the controller verifies that there are no disk status errors (such as offline, not ready, unsafe, write protect, offset active, or seek incomplete), seeks to the specified cylinder, and sets the specified head address. A verify ID and ECC is done after the seek. Relocation from a bad track to a spare track is allowed with the spare track being formatted. If the verify ID fails due to a data or search error, the track is formatted; however, the verify ID or search error is retried up to three times before formatting. The WRITE FORMAT command also returns ID error status if the ID is invalid and no ECC errors exist. If these errors are encountered during the verify ID, retries are returned. The controller assembles the ID words from its internal registers and counters and records the word(s) on the disk at the specified disk track address. The controller then records the data field following the ID words with the data word in the specified TILINE address. This is repeated for all data word positions and ECC. The controller formats each sector on the track with ID words, data, ECC, and the required gaps. Each sector has a physical data field of 128 words (256 bytes). All sectors contain ID words and the ECC field.

READ DATA COMMAND

The READ DATA command identifies a record location, specifies the number of bytes to be transferred from this location, and gives the starting address for the TILINE memory address buffer area to receive data from the disk.

After firmware initialization, the controller performs the following operations:

1. Checks for unit errors by examining the disk status bits (Offline, Offset Active, Not Ready, Unsafe, and Seek Incomplete).
2. Seeks to the specified cylinder.
3. Sets the specified head address.
4. Locates the desired sector by reading sectors into the sector buffer and checking the ID Words. If the Words contain the defective track bit (no ECC error existing), another SEEK is issued to the head and cylinder address specified in the data field, and the operation continues on the alternate track.
5. Transfers the Data Words to the specified TILINE address.

A failure to verify an ID Word results in an ID Error Status (bit 11) and termination of the Read Data operation. If the ECC is incorrect for the sector where data is being read, Data Error Status (bit 9) is also set. When the controller encounters the end of a sector, but the remaining Transfer Word is nonzero, the controller automatically continues reading data on the next sequential logical sector (if it exists). The controller automatically switches heads and/or cylinders, if necessary, to access the next logical sector.

When the remaining transfer word count is zero but the controller has not encountered the end of a sector, the controller discontinues transmitting Data Words across the TILINE. However, it does continue to read data from the disk until the end of the sector is encountered so that the ECC character can be checked before loading status.

When the controller encounters the end of a track and the remaining word count is nonzero, the controller automatically increments the head address to the next track. The controller then repeats steps 4 and 5 in the list above.

When the controller encounters the end of a cylinder and the remaining transfer count is nonzero (and head offset is not specified), the controller automatically seeks to the next cylinder and selects head address zero for the new track. The controller then repeats steps 4 and 5 in the list above.

WRITE DATA COMMAND

The WRITE DATA command causes the controller to record data on a previously formatted track, or to write over a previously recorded sector. After firmware initialization, the disk controller performs the following operations:

1. Checks for unit errors by examining disk status (Offline, Not Ready, Unsafe, Write Protect, Offset Active, or Seek Incomplete).
2. Seeks to the specified cylinder.
3. Selects the specified head address.
4. Locates the desired starting sector by reading the ID Words of each sector and comparing its contents to the desired sector address. If the Words contain the defective track bit and no ECC errors exist, another SEEK is issued to the head and cylinder address specified in the data field and the operation continues on the alternate track. When the controller detects the sector immediately before the desired sector, it arms the interface so that the Write operation is started when the next sector mark occurs.
5. Writes a leading gap, a synchronization character, header, 256 bytes of data from the specified TILINE memory location, and an ECC character. It also leaves a trailing gap at the end of the sector.

If the ID Words in step 4 do not compare, the Write operation is terminated with an ID status error.

Data is written on the disk, sector by sector, until the specified number of words have been transferred (unless a terminate condition is encountered). When the transfer word count is less than the sector word count, the controller fills the remainder of the sector with zeroes until the sector word count has been decremented to zero. When the number of words is greater than the words per sector, the controller continues to the next sequential sector.

When the controller encounters the end of a track and the remaining transfer word count is nonzero, the controller automatically increments the head address to the next track and selects sector 0 as the next sector to be written. The controller then repeats steps 4 and 5 of the list above.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, the controller automatically seeks to the next cylinder, selects head address zero for the new cylinder, and selects sector 0 as the next sector to be written. The controller then repeats steps 4 and 5 in the list above.

UNFORMATTED READ COMMAND

The UNFORMATTED READ command is included to insure compatibility with Texas Instruments' device service routines that acquire disk parameters by reading header information. This non-extended command does not actually read any data from the disk. Instead, three Words are returned to the CPU after this command is executed. The first Word returned contains the head and cylinder addressed, the second Word contains the number of sectors per record (Ø1), and the third Word contains the record word count (8Ø). If a genuine Unformatted Read operation is desired, the extended UNFORMATTED READ command may be used.

UNFORMATTED WRITE COMMAND

An UNFORMATTED WRITE command transfers up to 51Ø bytes of data from a specified TILINE address to a specified disk address. After firmware initialization, the controller seeks to the specified cylinder, selects the specified head address, detects the beginning of a sector, generates the correct lead gap, writes a sychronizaton character, and writes data on the disk. All data is written consecutively without regard to existing sector boundaries until the specified number of words has been transferred, or until a termination condition is encountered. The controller adds an ECC character and a trailing gap at the end of the data. The maximum transfer count is 51Ø bytes.

SEEK COMMAND

The SEEK command causes the drive to orient the heads at the cylinder specified in the Command Words. An interrupt may be generated, if desired, to alert the CPU that this operation has been completed.

If the heads are located on a common carriage assembly (as in the CMD disk drive), independent Seek operations cause the assembly to move all heads to the next specified recording or reading location and then return to the original track to finish the operation. This head thrashing is eliminated by ignoring (NOP) any pre-SEEK command from the software to the CMD disk drive.

On other types of drives not using a common carriage for two drive units, Seek operations are performed normally. If two or more of these drives are daisy chained, independent OVERLAPPED SEEK commands may be used.

RESTORE COMMAND

The RESTORE command re-initializes the cylinder counter and repositions the heads of the disk drive over cylinder zero. The RESTORE command is generally used to clear an Unsafe condition at the disk drive, but is required if Seek Incomplete or Unsafe status is detected. Before executing the Restore operation, the controller examines the Offline bit for a disk status error. If a disk status error is detected before the RESTORE command is initiated, the controller sets the Unit Error bit in Control Word 7. Completion of the Restore operation may be determined by enabling a disk drive completion interrupt (Attention bit interrupt), or by monitoring the Attention bit for the selected drive unit.

3.2.3 EXTENDED COMMAND DESCRIPTIONS

The extended commands set the Extended Mode bits (Control Word 1, bits 0 and 1). The extended mode bits allow the command code field (Control Word 1, bits 5-7) to select from an additional set of commands. These commands are less commonly used during the course of data storage and retrieval operations.

READ UNFORMATTED COMMAND

The extended READ UNFORMATTED command allows the programmer to read a sector and to examine a specified number of words starting immediately after the sync character without regard to ECC errors or standard sector formatting. This is primarily a diagnostic feature.

After firmware initialization, the controller selects the proper head and seeks to the specified cylinder. When the sector is located, the controller transfers the specified number of words to TILINE memory, starting with the first word after the sync character.

The ID words, data fields, ECC words, and trailing gap are read and transferred to memory as data words. There are normally glitches in the trailing gap due to write head turn-on and turn-off transients and differing write clock phases recorded during Formatting and Write operations. These glitches may cause shifting of word boundaries when the word count is large enough to require data to be written beyond the normal position of the ECC characters.

An ECC check is performed at the end of the operation, and data error status is reported if the ECC check shows an error. However, no ECC correction is attempted. A data error will occur unless the byte count is the correct value to allow a comparison between the calculated ECC checkbits and the read checkbits.

The word transfer count is limited to 510 bytes, and a command TIME-OUT occurs if too many bytes are requested. The extended READ UNFORMATTED command may also be used to read the information.

SELF-TEST COMMAND

This command causes the controller to execute Self-Test routines. The Self-Test routines are not individually selectable, but in order to maintain compatibility, the upper byte of Control Word 3 is copied into the lower byte of Control Word 2 upon successful completion of the SELF-TEST command.

ABSOLUTE WRITE FORMAT COMMAND (Revision B Firmware only)

The ABSOLUTE WRITE FORMAT command is non-relocatable. The controller checks for unit errors by examining disk status (Offline, Not Ready, Unsafe, Write Protect, Offset Active, or Seek Incomplete). It also seeks to the specified cylinder, sets the specified head address, waits for the correct starting sector, and formats the track with the fill word specified by the TILINE address. The format of this command is as follows:

- WORD 0: Always zero.
- WORD 1: Most significant byte = #C1, least significant byte = head address of the track.
- WORD 2: 0100.
- WORD 3: Cylinder address of the track.
- WORD 4: TILINE byte count = 0002.
- WORD 5: TILINE address.
- WORD 6: TILINE address and unit address.
- WORD 7: Always zero.

WRITE FORMAT FLAGGEDRevision A Firmware

For standard models of the SPECTRA 16/26 (except model M), the controller contains a switch-selectable Automatic Alternate Track feature. If the switch is disabled, the controller executes commands as described for the CD1400. If the switch is enabled, the alternate track feature allows alternate tracks to be assigned to defective tracks. It is invisible to the system software. The Drive Configuration PROM indicates the number of logical cylinders available to the system. The number of logical cylinders is equal to the number of physical cylinders minus the number of cylinders reserved for alternate tracks.

The formatter program must be rewritten to support this feature. The new formatter program is the only program that acknowledges the alternate cylinders. It performs a surface check on all physical cylinders and keeps a record of the defective tracks. At the end of the program, the defective tracks on any logical cylinder are assigned to good alternate tracks within the reserved cylinders. This occurs when the program issues a WRITE FORMAT command with the extended command bit set. (Write Format Flagged).

When the controller receives this command, it seeks to the specified cylinder and head in the "TILINE" control space and reads three words from memory. The words have the following meaning:

- WORD 0 : ALTERNATE CYLINDER ADDRESS
- WORD 1 : ALTERNATE HEAD ADDRESS
- WORD 2 : DATA FOR DATA WORDS 5-258

WRITE FORMAT FLAGGED [continued]

It will then format every sector on the track with the following format:

WORD 0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	CYLINDER ADDRESS																
WORD 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	0	HEAD ADDRESS							1	SECTOR ADDRESS							
WORD 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
WORD 3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	ALTERNATE CYLINDER ADDRESS																
WORD 4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	0	0	0	0	0	0	0	0	0	ALTERNATE HEAD							
WORD 5-258	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	DATA WORD FROM MEMORY																
WORDS 259-260	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	ECC FIELD GENERATED BY THE CONTROLLER																

Having formatted the defective track, the controller will seek to the alternate track and format it before terminating the command. The format of the first three words of every sector of the alternate track is as follows:

WORD 0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	ALTERNATE CYLINDER ADDRESS																
WORD 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	0	HEAD ADDRESS							0	SECTOR ADDRESS							
WORD 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

WORD 1, bit 8 = Defective track flag bit
WORD 1, bit 0 = Alternate track flag bit

WRITE FORMAT FLAGGED [continued]

If a normal READ or WRITE command is now issued to a track marked as defective, the controller reads the alternate information, seeks to the alternate track, and executes the command. On termination of a normal READ or WRITE command, the TILINE control space is the same as if no defective track existed.

If a normal READ or WRITE command is issued directly to the alternate track, the command fails and ID ERROR is set. The alternate track can be read indirectly via the defective track or with a READ UNFORMATTED EXTENDED command to the alternate track. The defective track must be read with a READ UNFORMATTED EXTENDED command.

The Drive Configuration PROM contains the number of cylinders in the drive minus those reserved for alternate tracks. Any even number from 0-30 may be reserved by having an appropriate value in the Configuration PROM. The STORE REGISTERS command reports the number of logical cylinders minus those assigned as alternates.

If the Automatic Alternate Track feature is disabled and the bad bit is detected, the controller reports an ID error in CONTROL WORD 7.

RELOCATE COMMAND (Revision B Firmware only)

If the alternate track switch is disabled, this command is performed as an ABSOLUTE WRITE FORMAT command. If the switch is enabled, the RELOCATE command is issued by the Surface Analysis program. The Surface Analysis program acknowledges the alternate cylinders by performing a surface check on all physical cylinders and keeping a record of the defective tracks. At the end of the program, the defective tracks on any logical cylinders are assigned to good alternate tracks within the reserved cylinders by using the RELOCATE command. The format of this command is as follows:

- WORD 0: Always zero.
- WORD 1: Most significant byte = 41_{16} , least significant byte = head address of the bad track.
- WORD 2: Always 0.
- WORD 3: Cylinder address of the bad track.
- WORD 4: TILINE byte count = 0004_{16} .
- WORD 5: TILINE address.
- WORD 6: TILINE address and unit address.
- WORD 7: Always zero.

After verifying the ID of the bad track, the RELOCATE command reads two words from memory. These words are shown below.

WORD 0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	ALTERNATE HEAD					ALTERNATE CYLINDER										

WORD 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	DATA WORD TO FORMAT ALTERNATE TRACK															

The RELOCATE command then formats sectors on the defective track with the following format.

WORD 0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	CYLINDER ADDRESS															

WORD 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	HEAD ADDRESS								SECTOR ADDRESS							

WORD 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WORD 3-258	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	ALTERNATE HEAD					ALTERNATE CYLINDER										

WORDS 259-260	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	ECC FIELD GENERATED BY THE CONTROLLER															

RELOCATE COMMAND [continued]

Having formatted the defective track, the controller seeks to the alternate track and formats it before terminating the command. The format of the alternate track is as follows.

WORD 0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	DEFECTIVE CYLINDER ADDRESS															
WORD 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	BAD HEAD ADDRESS	SECTOR ADDRESS														
WORD 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WORD 3-258	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	DATA WORD FROM MEMORY															
WORDS 259-260	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ECC FIELD GENERATED BY THE CONTROLLER															

If a normal READ or WRITE command is now issued to a track marked as defective, the controller reads the alternate information, seeks to the alternate track, and executes the command. On termination of a normal READ or WRITE command, the TILINE control space is the same as if no defective track existed.

If a normal READ or WRITE command is issued directly to the alternate track, the command fails and ID ERROR is set. The alternate track can be read indirectly via the defective track or with a READ UNFORMATTED EXTENDED command to the alternate track. The defective track must be read with a READ UNFORMATTED EXTENDED command.

The Drive Configuration PROM contains the number of cylinders in the drive minus those reserved for alternate tracks. Any even number from 0-30 may be reserved by having an appropriate value in the Configuration PROM. The STORE REGISTERS command reports the number of logical cylinders minus those assigned as alternates.

If the Automatic Alternate Track feature is disabled and the bad bit is detected, the controller reports an ID error in CONTROL WORD 7.

3.2.4 COMMAND COMPLETION

Upon completion of an operation, the controller will generate an interrupt to the CPU if the Interrupt Enable (IE) bit in Control Word 7 is set. The SPECTRA 16/26 controller may be used with either an interrupt driven or a polled device service routine.

Command Completion Without Interrupts

To check command completion or controller availability in a polled system, it is necessary to read Control Word 7 periodically to check bit 0 for idle status. If the bit is set, it indicates that the controller is idle and available to accept commands; if the bit is reset, it indicates that the controller is busy.

When controller operation begins, the software initiates a timing loop and checks the Idle bit at timer expiration. If the idle bit is still zero, the timer may be restarted and the sequence may be repeated a preselected number of times. This method requires more software overhead than the interrupt driven approach.

If a RESTORE or INDEPENDENT SEEK command is initiated, the disk may not be ready even after the controller has reported completion. To determine if the disk has completed a RESTORE or INDEPENDENT SEEK command, the software should check the drive status bits of Control Word 0. If the disk drive has finished the operation, the attention line for the selected drive will be set, and either the Not Ready bit will be inactive or the Seek Incomplete bit will be set. The Independent Seek operation is intended for use with SMD type drives, not with QMD type drives.

Command Completion With Interrupts

The controller may issue two types of interrupts to the computer. One type of interrupt is issued when the controller completes a command, and the other type is issued when the disk drive completes an operation. Most disk drive operations are completed when the controller has completed a command. For independent Seek and Restore operations, however, the controller completes the command before the drive completes the operation. The drive completion interrupt may then be used to determine when the system is again ready.

In order to have the controller issue an interrupt to the processor upon command completion, the Interrupt Enable (IE) bit in Control Word 7 must be set when the operation is initiated. When the controller returns to idle, the interrupt is issued to the CPU. This interrupt is cleared by resetting the IE bit or the appropriate completion bit in Control Word 7.

Drive completion interrupts are issued when the attention bit and mask bit for any disk drive unit are both set, setting the interrupt line to the computer. Control Word 0 contains four attention lines (one for each of the four disk drive unit addresses) and four attention mask lines. Each drive's attention line is set when either the disk drive is ready or a seek error has occurred.

Command Completion With Interrupts [continued]

The mask bits may be set or reset using any of the computer memory instructions. However, the attention bits and disk status bits are set only by the controller, to indicate current disk operation status.

To use the drive completion interrupts during a Restore operation, first issue the RESTORE command to the controller. After the controller reports command completion (by a controller Idle or command completion interrupt), set the mask bit corresponding to the desired drive. When the drive finishes the Restore operation and the controller is idle, an interrupt is issued to the CPU. The interrupt may be cleared by resetting the mask bit corresponding to the interrupting drive. The controller resets all controller interrupts when it switches from an idle to a busy condition.

3.3 DISK FORMAT

Sector Format: (CD1400 and DS80)

GAP 1	SYNC	ID	DATA	ECC	END GAP
-------	------	----	------	-----	---------

<u>FIELD</u>	<u>CONTENTS</u>
GAP 1	35 bytes of zeroes.
SYNC	2 bytes, hexadecimal A7CC.
ID	6 bytes containing head, cylinder, and sector addresses, plus a flagged track indicator.
DATA	256 bytes of system data.
ECC	4 bytes of Error Correction Code.
END GAP	A variable number of bytes per sector (usually 12).

CD1400 COMPATIBLE DISK FORMAT

The ID field used to perform position verification and flag tracks has the following format:

ID WORD 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL

BIT	NAME	FUNCTION
0-4	-----	Not used. Always zero.
5	CYL Cylinder Address MSB	This bit is to be used with Ampex 160 MB drives or the equivalent as the 1024 weight cylinder bit.
6-15	CYL Cylinder Address	These bits contain the cylinder address which ranges from 0-1023. Bit 15 is the Least Significant Bit. The maximum address range with bit 5 is 2047.

ID WORD 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AT	HA	HA	HA	HA	HA	HA	HA	FT	SA	SA	SA	SA	SA	SA	SA

BIT	NAME	FUNCTION
0	AT Alternate Track	This bit specifies the alternate track.
1-7	HA Head Address	These bits contain the head address.
8	FT Flagged Track	This bit is used with the Automatic Alternate Track feature to indicate the track is flagged defective.
9-15	SA Sector Address	These bits contain the sector address.

ID WORD 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
0-15	---	Not used. Always zero.

DS80 COMPATIBLE DISK FORMAT

The ID field used to perform position verification and flag tracks has the following format:

ID WORD 0

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL	CYL

BIT	NAME	FUNCTION
0-4	-----	Not used. Always zero.
5	CYL Cylinder Address MSB	This bit is to be used with Ampex 160 MB drives or the equivalent as the 1024 weight cylinder bit.
6-15	CYL Cylinder Address	These bits contain the cylinder address which ranges from 0-1023. Bit 15 is the Least Significant Bit. The maximum address range with bit 5 is 2047.

ID WORD 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HA	HA	HA	HA	HA	HA	HA	HA	SA	SA	SA	SA	SA	SA	SA	SA

BIT	NAME	FUNCTION
0-7	HA Head Address	These bits contain the head address.
8-15	SA Sector Address	These bits contain the sector address.

ID WORD 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BTF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
0	BTF Bad Track Flag	When set, this bit indicates that a defective track has been reallocated to an alternate track. The alternate head and cylinder address is recorded in the following data field.
1-15	-----	Not used. Always zero.

DISK FORMAT (Trident compatible Model M)

GAP 1	SYNC	ID	DATA	ECC	END GAP
-------	------	----	------	-----	---------

<u>FIELD</u>	<u>CONTENTS</u>
GAP 1	35 bytes of zeroes.
SYNC	1 byte, hexadecimal 01.
ID	8 bytes containing logical head and cylinder address, record word count, sectors per record, sector address, and physical head number.
DATA	288 bytes of system data.
ECC	4 bytes of Error Correction Code.
END GAP	A variable number of bytes per sector (usually 12).

The ID field used to perform position verification and flag tracks has the following format:

ID WORD 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HA	HA	HA	HA	HA	HA	HA	HA	CA	CA	CA	CA	CA	CA	CA	CA

BIT	NAME	FUNCTION
0-7	HA Head Address	These bits specify the logical head address.
8-15	CA Cylinder Address	These bits specify the logical cylinder address.

ID WORD 2

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC

BIT	NAME	FUNCTION
0-15	RWC Record Word Count	These bits specify the record word count.

ID WORD 3

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SR	SR	SR	SR	SR	SR	SR	SR	SA	SA	SA	SA	SA	SA	SA	SA

BIT	NAME	FUNCTION
0-7	SR Sectors/Record	These bits specify the number of sectors per record.
8-15	SA Sector Address	These bits specify the sector address.

ID WORD 4

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HN	HN	HN	HN	HN	HN	HN	HN	HN	HN	HN	HN	HN	HN	HN	HN

BIT	NAME	FUNCTION
0-15	HN Head Number	These bits specify the physical head number.

3.4 INTERLEAVING

The SPECTRA 16/26 interleaves sectors 3 to 1 in a standard configuration. For increased performance, the controller is also capable of interleaving 1 to 1 for contiguous sectors, or 2 to 1 provided that the total number of sectors per track is odd.

The following algorithms are used to calculate the format to be written on the disk.

3:1 Interleaving

Divide the total number of sectors per track (S) by 3.

If the remainder = 2, set $i = S/3 + 1$.

If the remainder = 1, set $i = 2S/3 + 1$.

If the remainder = 0, set $i = 1$.

The logical sector addresses after index are calculated as shown below, where h = logical head number and S = the number of sectors per track.

The first logical sector address = $FSEC = (i-1) - h(i+1)$ modulo S .

The second logical sector address = $FSEC + i$ modulo S .

The third logical sector address = $FSEC + 2i$ modulo S .

The fourth logical sector address = $FSEC + 3i$ modulo S .

If the number of sectors per track is exactly divisible by three and the remainder is zero, setting $i = 1$ causes the sectors to be contiguous instead of interleaved 3 to 1.

EXAMPLE

3 : 1 interleaving with 64 sectors per track:

$64/3 = 21$ remainder 1

$i = 42 + 1 = 43$

For head 0, $FSEC = (43-1) - 0(43+1)$ modulo 64 = 42

For head 1, $FSEC = (43-1) - 1(43+1)$ modulo 64 = 62

The logical sector addresses after index are:

For head 0: 42, 21, 0, 43, 22, 1, 45, 23, 2, etc.

For head 1: 62, 41, 20, 63, 42, 21, 0, 43, 22, 1, etc.

2 : 1 INTERLEAVING

Divide the total number of sectors per track (S) by 2.

If the remainder = 1, set $i = S/2 + 1$.

If the remainder = 0, set $i = 1$.

The logical sector addresses after index are calculated as shown below, where h = logical head number and S = the number of sectors per track.

The first logical sector address = FSEC = $(i-1) - h(i+1)$ modulo S .

The second logical sector address = FSEC + i modulo S .

The third logical sector address = FSEC + $2i$ modulo S .

If the number of sectors per track is exactly divisible by two and the remainder is zero, setting $i = 1$ causes the sectors to be contiguous instead of interleaved 2 to 1.

EXAMPLE

2 : 1 interleaving with 61 sectors per track:

$61/2 = 30$ remainder 1

$i = 30 + 1 = 31$

For head 0, FSEC = $(31-1) - 0(31+1)$ modulo 61 = 30

For head 1, FSEC = $(31-1) - 1(31+1)$ modulo 61 = 59

The logical sector addresses after index are:

For head 0: 30, 0, 31, 1, 32, 2, 33, 3, 34, etc.

For head 1: 59, 29, 60, 30, 0, 31, 1, 32, 2, 33, etc.

1 : 1 INTERLEAVING

For 1 : 1 interleaving, set $i = 1$ and the same formulas apply.

EXAMPLE

1 : 1 interleaving with 64 sectors per track:

For head 0, FSEC = $(1-1) - 0(1+1)$ modulo 64 = 0.

For head 1, FSEC = $(1-1) - 1(1+1)$ modulo 64 = 62.

The logical sector addresses after index are:

For head 0: 0, 1, 2, 3, 4, 5, etc.

For head 1: 62, 63, 0, 1, 2, 3, etc.

The head skew seen here is necessary to allow the controller time to select a new head when a multiple sector transfer crosses a track boundary.

3.5 TAPE REGISTER DEFINITIONS

The control and status words described in this section are used to control tape operations and to report tape status. A summary of these words is shown below.

CONTROL WORD 0

TAPE TRANSPORT STATUS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	BOT	EOR	EOF	EOT	WP	TR	CTO	TRW	TRW	TRW	TRW	RWM	RWM	RWM	RWM

CONTROL WORD 1

READ OVERFLOW STATUS COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC

CONTROL WORD 2

READ OVERFLOW STATUS COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	RES	RES	RES	RES	RES	RES	RES	RES

CONTROL WORD 3

READ OFFSET

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS

CONTROL WORD 4

CHARACTER COUNT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC

CONTROL WORD 5

BUFFER ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA

CONTROL WORD 6

COMMAND AND TRANSPORT SELECT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
US	US	US	US	CMC	CMC	CMC	CMC	WD	0	0	MBA	MBA	MBA	MBA	MBA

CONTROL WORD 7

TMTC STATUS AND CONTROL

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	OC	ERR	IE	LO	RSV	PE	AC	VRC	ECC	HE	MER	TE	TOE	FE	TER

CONTROL WORD 0 TAPE TRANSPORT STATUS

This word contains tape transport status.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OFL	BOT	EOR	EOF	EOT	WRP	TR	CTO	TRW	TRW	TRW	TRW	RWM	RWM	RWM	RWM

BIT	NAME	FUNCTION
0	OFL Offline	When set, this bit indicates that the selected drive is not ready and unavailable for any tape commands.
1	BOT Beginning Of Tape	When set, it indicates that the tape is positioned at the load point.
2	EOR End Of Record	This bit is set when an inter-record gap is encountered.
3	EOF End Of File	This bit is set when a file mark is read. Error and Tape Error are also set.
4	EOT End Of Tape	Set when the tape is positioned at or beyond the end of the tape reflective strip. Reset when the tape passes over the strip in reverse under program control.
5	WP Write Protected	Set if the drive is write protected and status is read. Error and Tape Error are also set.
6	TR Tape Rewind	Set when the tape drive reaches End Of Tape and the drive proceeds to rewind.
7	CTO Command Time Out	Set if the controller fails to complete an operation before the command timer expires.
8-11	TRW Transport Rewinding	When the appropriate bit is set, it indicates that the corresponding tape drive is rewinding.
12-15	RWM Rewind Mask	When the appropriate bit is set, it enables a rewind complete interrupt for the corresponding tape drive.

CONTROL WORD 1 READ OVERFLOW STATUS COUNT

This word contains the read overflow count.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC

BIT	NAME	FUNCTION
0-15	ROC Read Overflow Count	These bits contain the lower 16 bits of the 24-bit read overflow count. Bit 0 is the most significant bit.

CONTROL WORD 2 READ OVERFLOW STATUS COUNT

This word contains the read overflow count.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROC	ROC	ROC	ROC	ROC	ROC	ROC	ROC	RES	RES	RES	RES	RES	RES	RES	RES

BIT	NAME	FUNCTION
0-7	ROC Read Overflow Count	These bits contain the upper 8 bits of the 24-bit read overflow count. Bit 7 is the least significant bit.
8-15	RES Reserved	These bits are reserved.

CONTROL WORD 3 READ OFFSET

This word is used by the processor to specify the read offset.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS	ROS

BIT	NAME	FUNCTION
0-15	ROS Read Offset	These bits specify the number of characters to read before starting a data transfer to memory.

CONTROL WORD 4 CHARACTER COUNT

This word is used for read character count, write character count, skip record count, or erase length.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC

BIT	NAME	FUNCTION
0-15	CC Character Count	The function of these bits is determined by the command code in word 6, bits 7-4. The contents are decremented as each character is read. If an error occurs, these bits contain the remaining number of bytes not read. During a Write operation, these bits determine the number of bytes not written. A SKIP RECORD COUNT command decrements the count for each record skipped, and an ERASE LENGTH command specifies the length of tape that is to be erased.

CONTROL WORD 5 BUFFER ADDRESS

This word contains the 15 least significant bits of the 20-bit TILINE memory buffer starting address.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA	MBA

BIT	NAME	FUNCTION
0-15	MBA Memory Buffer Address	Bits 14-0 are the 15 least significant bits of the 20-bit TILINE starting memory address. The 5 most significant bits are contained in word 6. Bit 15 is always zero.

CONTROL WORD 6 COMMAND AND TRANSPORT SELECT

This word contains command codes and selects one of four possible tape transport units.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
US	US	US	US	CMC	CMC	CMC	CMC	WD	0	0	MBA	MBA	MBA	MBA	MBA

BIT	NAME	FUNCTION
0-3	US Unit Select	These bits select one of the four possible logical tape units. If a command is issued without a unit select bit set, the tape interface will be reset and the command will terminate with "Command Timeout".
4-7	CMC Command Codes	These bits select the operation to be performed. The command codes are defined in table 3-2.
8	WD Write Diagnostic	When set, this bit forces a parity error on a Write. This causes the drive to pulse the Hard Error signal on the tape interface.
9-10	----	These bits are reserved for diagnostics. Always zero.
11-15	MBA Memory Buffer Address	Bits 15-11 are the 5 most significant bits of the 20-bit TILINE starting memory address.

TABLE 3-2 COMMAND CODES

BIT 4	BIT 5	BIT 6	BIT 7	COMMAND
Ø	Ø	Ø	Ø	NOP
Ø	Ø	Ø	1	NOP
Ø	Ø	1	Ø	WRITE EOF
Ø	Ø	1	1	RECORD SKIP REVERSE
Ø	1	Ø	Ø	READ BINARY
Ø	1	Ø	1	RECORD SKIP FORWARD
Ø	1	1	Ø	WRITE BINARY
Ø	1	1	1	ERASE
1	Ø	Ø	Ø	READ STATUS
1	Ø	Ø	1	READ STATUS
1	Ø	1	Ø	REWIND
1	Ø	1	1	REWIND AND UNLOAD
1	1	Ø	Ø	NOP
1	1	Ø	1	NOP
1	1	1	Ø	NOP
1	1	1	1	NOP

CONTROL WORD 7 TMTc STATUS AND CONTROL

This word contains control bits from the processor and status information from the tape controller.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
IDL	OC	ERR	IE	LO	RSV	PE	AC	VRC	ECC	HE	MER	TE	TOE	FE	TER

BIT	NAME	FUNCTION
0	IDL Idle	When set, the controller is not busy. If a command is used when Idle is 0, the controller ignores the command.
1	OC Operation Complete	Set at the error-free completion of an operation.
2	ERR Error	Set when an operation is terminated due to error.
3	IE Interrupt Enable	When set, this bit enables the controller to generate an interrupt when Operation Complete or Error is set.
4	LO Lock Out	This bit is set when Control Word 7 is read.
5	-----	Reserved for diagnostics. Always zero.
6	PE PE Format	Set if the transport is in PE format (1600 bpi).
7	AC Abnormal Completion	This bit is set if a tape operation is terminated due to an I/O reset or power fail warning.

CONTROL WORD 7 TMIC STATUS AND CONTROL [continued]

BIT	NAME	FUNCTION
8	VRC Vertical Redundancy Check	This bit is set if the controller detected a Read Data Parity error.
9	ECC Error Correction Enabled	The setting of this bit is determined by the type of transport selected. For an NRZI transport, this bit is a longitudinal Redundancy Check (LRC) error indicator. For a PE format, this bit indicates that ECC is enabled and a single bit correction has been performed.
10	HE Hard Error	This bit is a CRC error indicator for an NRZI drive. For a PE drive, this bit is set if one of the following errors is detected during a Read Binary Forward operation: No PE mark, Multitrack dropout error, False postamble error, or a Skew error. See the table below.
11	MER Memory Error	Set if a memory Read error is detected during a data transfer operation. ERR is also set.
12	TE TILINE Timing Error	When set indicates that a timing error has occurred because the TILINE could not keep up with the controller during a data transfer operation.
13	TOE TILINE Time- out Error	Set if a transfer cycle is not completed in 10 microseconds after the controller gains TILINE access. May occur when attempting to access non-existent memory.
14	FE Format Error	Not used. Always zero. (NRZI format).
15	TER Tape Error	This bit is set if a transport error has occurred.

3.5.1 COMMAND DESCRIPTIONS

The command code which selects the operation to be performed by the controller is formed by bits 4-7 of Control Word 6. The command code assignments are shown in the description of Word 6, and the tape commands are described below.

NO OPERATION COMMAND

When a NO OPERATION (NOP) command is issued, the controller responds by setting Idle and Operation Complete status (Control Word 7, bits 0 and 1).

WRITE END-OF-FILE

The WRITE END-OF-FILE command causes a file mark to be written on the tape. The controller checks the EOF mark after writing it on the tape. An error will be reported as a VRC error (Control Word 7, bit 8) by an NRZI tape drive, or as a PE hard error (Control Word 7, bit 10) by a PE tape drive.

RECORD SKIP REVERSE

The RECORD SKIP REVERSE command causes the tape to pass over the heads in the reverse direction without transferring data to memory. The number of records to be skipped is specified in Control Word 4, and the contents of that Word are decremented each time a record is skipped.

READ BINARY FORWARD

The READ BINARY FORWARD command reads data from tape and transfers it to main memory. The controller acquires control of the TILINE, assembles the tape characters into 16-bit words, and transmits the words into successive memory locations.

SKIP RECORD FORWARD

The SKIP RECORD FORWARD command causes the tape to skip over records without transferring any data to memory. The number of records to be skipped is loaded into Control Word 4, which is decremented each time a record is skipped. If the initial record number is zero, the controller attempts to skip 65,536 records and stops on EOT or EOF.

WRITE BINARY FORWARD

The WRITE BINARY FORWARD command reads data from main memory via the TILINE and records it on tape. The 20-bit starting address of the memory buffer is specified in Control Word 6 (bits 11-15) and Control Word 5 (bits 0-14). The number of 8-bit characters to be recorded is specified in Control Word 4.

ERASE

The ERASE command erases a measured length of tape. Control Word 4 is loaded with the value "K" from which the length (L) is determined as follows:

NRZI transport: $L \text{ (inches)} = 0.666 + K(0.00125)$. Maximum length = 81.92 inches.

PE transport: $L \text{ (inches)} = 0.666 + K(0.000625)$. Maximum length = 42.6 inches.

READ STATUS

The READ STATUS command selects a transport and returns transport status information without performing any transport functions. The controller responds to the command by returning a transport status word (Control Word 0) and a controller status word (Control Word 7).

REWIND

The REWIND command checks the selected transport to see if it is already rewinding. If it is not rewinding, the controller commands the transport to rewind, and reports Idle and Operation Complete in Control Word 7. If the selected transport is already rewinding, the controller reports Idle, Error and Tape Error (Control Word 7, bits 0, 2, and 15), and the tape rewinding status (Control Word 0, bit 6).

REWIND AND UNLOAD

The REWIND AND UNLOAD command causes the tape to rewind and unload from the transport. It also causes the Offline bit to be set.

Chapter Four

Diagnostics

4.1 DISK DIAGNOSTIC PROGRAMS

This chapter explains the diagnostic programs that may be used to check out the disk subsystem when connecting the SPECTRA 16/26 controller to a particular drive. The disk diagnostics supplied by TI are:

DSKSA	SURFACE ANALYSIS TEST
DSKCD1	CDD CONTROLLER/DISK DIAG PART 1
DSKCD2	CDD CONTROLLER/DISK DIAG PART 2
DSKCOM	COMMON CONTROLLER/DISK

NOTE: The above diagnostics must include WD900 disk types for WD900 emulation.

The first program that should be run is DSKSA to format the whole disk. Use the verb FD to format the system part of the disk, and the verb FC to format the diagnostic cylinders. The two other diagnostics may be run in any order. Depending upon the disk type chosen and the drive attached, the diagnostics may need to be patched. If the DS80 disk type is chosen, 10 alternate tracks are used. If the WD900 disk type is chosen, 16 alternate tracks are used. If the CD1400 disk type is chosen, no alternate tracks are used.

If the selected drive parameters are not compatible with the selected disk type, three locations must be patched using the following procedure:

After loading the diagnostic and answering the "IT" questions, run the subsequent list of verbs.

-Reference appropriate notes on the following pages.

(The drive used in the following example is a Fujitsu 2351).

```

VERB? SR <CR>
STORE REGISTERS
*** ERROR 001B DSKSA XR
STORE REGISTER VALUES DIDN'T AGREE WITH THE DISK TYPE ENTERED DURING "IT".
EXPECTED VALUES FOR A DS80
WORD 1=1E80 WORD 2=3D00 WORD 3=2B35
RECEIVED VALUES FOR AN UNDEFINED DISK TYPE
WORD 1=2C00 WORD 2=5800 WORD 3=533E

```

(Note 1)

```

VERB? .MS <CR>
COND (EQ NE GT LT DEF=EQ) EQ <CR>
ADDRESS (000000) 6000 <CR>
# OF WORDS (DEF=0000) 9000 <CR> DATA (DEF=0000) 2B35 <CR> (Note 2)
0072CD=2B35 (Note 3)

```

```

VERB? .MM <CR>
ADDRESS (000000) 0072B6 <CR>
0072E6 - 1E80 - 2C00 <CR>
0072E8 - 3D00 - 5800 <CR>
0072EA - 2B35 - 533E <CR>
0072EC - 3200 - <CMD>
VERB? ____ (Patching is complete)

```

Note 1: Verify that the "received values for undefined disk type" are the values required for selected disk drive. (See Disk Drive Configuration Store Register Tables).

Note 2: Always input data EQUAL to word 2 (Head Cylinder) to be sure the correct drive type was selected for patching. Then subtract a hex 4 from the selected address.

Example: >72C0 - >4 = >72BC

Use this value for .MM

Note 3: Address values will be different with each revision level and each diagnostic used.

4.2 DIAGNOSTIC TESTING ERRORS

Certain errors may be encountered; these errors are shown as follows.

DSKCD1 TEST 31 - Quick Disk Test	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M on.
DSKCD1 TEST 41 - Command Verification	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M on.
DSKCD1 TEST 56 - Rate Error Test	Fails because the buffer prevents this error from occurring.
DSKCD1 TEST 58 - Search Error Test	Fails due to format differences if sectors are not interleaved 3 to 1.
DSKCD2 TEST 21 - Interlace Timing Test	May fail if the motor RPM is not 3600, if a burst count other than 1 has been selected, or if contiguous sectors are being used.
DSKCD2 TEST 22 - Motor RPM Test	May fail if the motor RPM is not 3600.
DSKCD2 TEST 31 - Interactive Test	Fails when switching the drive on-line when the program expects to see the unsafe bit set.
DSKCOM TEST 23 - Jitter Address Test	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M on.
DSKCOM TEST 24 - Random Read Test	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M on.
DSKCOM TEST 62 - Short Exerciser	Fails due to format differences when testing the fixed portion of a CMD or DFR with switch 5 of 9M on.

4.3 MAG TAPE DIAGNOSTICS

The TI 979 diagnostic "TAPTST" may be run on the SPECTRA 26/36. Some failures must be expected due to the different characteristics of the tape drive being used and the TI 979 tape drive. The following table gives a list of failures when running the diagnostic TAPTST, version B.

<u>TEST</u>	<u>FAILURE</u>
A,B	Fails because the diagnostic expects a VRC error after a diagnostic write. The controller will force bad parity on a diagnostic write, but will only report Hard Error.
C	Fails on some NRZ transports due to different ramp times.
10	Fails forward creep test on some transports due to different transport characteristics.
15	Fails the rewind and unload test on transports which do not support rewind and unload, and fails on transports which do not go off line until after they have rewound to BOT.

4.4 MICRODIAGNOSTICS

Microdiagnostics are run each time the controller powers up. There are three LEDs on the SPECTRA 16/26 that show the status of the controller. The red LED indicates that the microdiagnostics have failed on power up. The two green LEDs indicate that both the disk and tape portions of the controller are idle.

The following table gives a list of possible combinations of these lights after power up.

<u>GREEN LED (MT)</u>	<u>GREEN LED (DK)</u>	<u>RED LED (DG BAD)</u>	<u>MEANING</u>
ON	ON	OFF	Microdiagnostics Successful.
OFF	ON	OFF	Disk portion of microdiagnostics successful. Ensure that W10 is installed.
OFF	OFF	OFF	LED failure.
OFF	OFF	ON	Microdiagnostics failure.
OFF	ON	ON	Microdiagnostics failure.
ON	ON	ON	LED failure.
ON	OFF	ON	LED failure.
ON	OFF	OFF	LED failure.

MICRODIAGNOSTIC FAILURE

For further information concerning microdiagnostic failure, see Words 2 and 4 of the disk register definitions. Words 2 and 4 have the following meanings.

<u>WORD 2</u>	<u>WORD 4</u>	<u>MEANING</u>
0000	0000	Diagnostics successful.
00XX	0000	Self-test command successful.
XX1X	XXXX	CSRC or CDEST bus failed.
F121	XXXX	CPU processor ALU failed logical test.
F222	XXXX	CPU processor ALU failed arithmetic test.
F323	XXXX	CPU processor ALU failed shift test.
F333	XXXX	CPU processor failed register address test.
F434	XXXX	CPU processor count failed.
F242	XXXX	CPU processor failed sector buffer pattern test.
F141	XXXX	CPU processor failed JSR/RTS test.
F343	XXXX	CPU processor INH CLK signal failed.
F444	XXXX	CPU processor MDAC signal failed.
F151	XXXX	CPU processor TIGO signal failed.
F353	XXXX	CPU processor WRN signal failed.
F454	XXXX	CPU processor NMTO signal failed.
F555	XXXX	CPU processor NMPE signal failed.
F181	XXXX	CPU processor/MT sequencer handshake failed.
F282	XXXX	MT FIFO full/empty not properly detected.
F383	XXXX	MT FIFO data failed.
F484	XXXX	MT data late or parity error detection failed.
F585	XXXX	MT timer test failed.
FF14	XXXX	CPU processor/Disk processor handshake failed.
FF15	XXXX	CPU processor INH CLK signal failed.
0000	1XXX	DSRC or DDEST bus failed.
0000	XX1X	DSRC or DDEST bus failed.
0000	2121	Disk processor ALU failed logical test.
0000	2222	Disk processor ALU failed arithmetic test.
0000	2323	Disk processor ALU failed shift test.
0000	3333	Disk processor ALU failed register address test.
0000	4141	Disk processor failed JSR/RTS test.
0000	4242	Disk processor failed serializer/deserializer data test.
0000	4343	Disk processor detected word available signal early.
0000	4444	Disk processor did not detect a word available signal.
0000	4545	Disk processor failed sync word detection test.
0000	5151	Disk processor ECC test failed.
0000	5252	Disk processor ECC error not detected.
0000	5353	Disk processor ECC error could not be reset.
0000	5454	Disk processor did not detect a word available signal.
0000	6161	Disk processor failed sector buffer upper byte test.
0000	6262	Disk processor failed sector buffer lower byte test.
0000	AAAA	Disk processor did not set ATTN at the end of its microdiagnostics.

APPENDIX

A,B,C,D

TAPE INTERFACE PLUG CONNECTIONS

CONTROLLER CONNECTOR J6

The tape interface is compatible with the Pertec industry standard embedded formatter. This interface consists of two 50 pin connectors with pin assignments and signals defined below.

<u>Live Pin</u>	<u>Ground</u>	<u>Signal Function</u>	<u>Signal Name</u>
2	1	Formatter Busy	FBY
4	3	Last Word	LWD
6	5	Write Data 4	W4
8	7	Initiate Command	GO
10	9	Write Data 0	W0
12	11	Write Data 1	W1
14	13	Reserved	RES
16	15	Reserved	RES
18	17	Reverse	REV
20	19	Rewind	REW
22	21	Write Data Parity	WP
24	23	Write Data 7	W7
26	25	Write Data 3	W3
28	27	Write Data 6	W6
30	29	Write Data 2	W2
32	31	Write Data 5	W5
34	33	Write	WRT
36	35	Reserved	RES
38	37	Edit	EDIT
40	39	Erase	ERASE
42	41	Write Filemark	WFM
44	43	Reserved	RES
46	45	Transport Address 0	TAD0
48	47	Read Data 2	R2
50	49	Read Data 3	R3

TAPE INTERFACE PLUG CONNECTIONS

CONTROLLER CONNECTOR J7

<u>Live Pin</u>	<u>Ground</u>	<u>Signal Function</u>	<u>Signal Name</u>
1	-	Read Data Parity	RP
2	-	Read Data 0	R0
3	-	Read Data 1	R1
4	-	Load Point	LDP
6	5	Read Data 4	R4
8	7	Read Data 7	R7
10	9	Read Data 6	R6
12	11	Hard Error	HER
14	13	Filemark	FMK
16	15	Identification 1	CCG
18	17	Formatter Enable	FEN
20	19	Read Data 5	R5
22	21	End Of Tape	EOT
24	23	Rewind/Unload	OFL
26	25	Reserved	RES
28	27	Ready	RDY
30	29	Rewinding	RWD
32	31	File Protect	FPT
34	33	Read Strobe	RSTR
36	35	Write Strobe	WSTR
38	37	Data Busy	DBY
40	39	Hi Speed Select Monitor	SPEED
42	41	Corrected Error	CER
44	43	On Line	ONL
46	45	Transport Address 1	TAD1
48	47	Formatter Address	FAD
50	49	High Speed Select	HISP

DISK INTERFACE PLUG CONNECTIONS

The disk interface is industry standard SMD compatible allowing attachment of up to four drives. The SPECTRA 16/26/36 provides an SMD compatible flat cable connector set with pin assignment and signals defined below.

"B" CABLE

J1, J2, J7, J8 CONNECTORS	CDC PIN #		SLC PIN #	
	LO	HI	-	+
Signal				
Write Data	8	20	15	14
Ground	7		13	
Write Clock	6	19	11	12
Ground	18		10	
Servo Clock	2	14	3	2
Ground	1		1	
Read Data	3	16	5	6
Ground	15		4	
Read Clock	5	17	9	8
Ground	4		7	
N/C	10	23	19	20
Unit Selected	22	9	18	17
Ground	21		16	
Reserved for Index	12	24	23	22
Ground	11		21	
Reserved for Sector	13	26	25	26
Ground	25		24	

NOTE: The 26 conductor shielded flat cable has a maximum length of 50 feet.

DISK INTERFACE PLUG CONNECTIONS"A" CABLE

J3 CONNECTOR	CDC PIN #		SLC PIN #	
	LO	HI	-	+
Signal				
Unit Select Tag	22	52	43	44
Unit Select 2(0)	23	54	45	46
Unit Select 2(1)	24	54	47	48
Unit Select 2(2)	26	56	51	52
Unit Select 2(3)	27	57	53	54
Tag 1	1	31	1	2
Tag 2	2	32	3	4
Tag 3	3	33	5	6
Bit 0	4	34	7	8
Bit 1	5	35	9	10
Bit 2	6	36	11	12
Bit 3	7	37	13	14
Bit 4	8	38	15	16
Bit 5	9	39	17	18
Bit 6	10	40	19	20
Bit 7	11	41	21	22
Bit 8	12	42	23	24
Bit 9	13	43	25	26

DISK INTERFACE PLUG CONNECTIONS"A" CABLE

J3 CONNECTOR	CDC PIN #		SLC PIN #	
	LO	HI	-	+
Signal				
Open Cable Detector	14	44	27	28
Index	18	48	35	36
Sector	25	55	49	50
Fault	15	45	29	30
Seek Error	16	46	31	32
On Cylinder	17	47	33	34
Unit Ready	19	49	37	38
Address Mark	20	50	39	40
Write Protect	28	58	55	56
Power Sequence Pick		29		57
Power Sequence Hold		59		58
Busy *1	21	51	41	42
Bit 10 *2	30	60	59	60

*1 Dual Port Unit only

*2 Bit 10 used for cylinder 1024

SPECTRA 26T DATA CHAINING

In addition to performing standard tape operations, the SPECTRA 26T also supports data chaining operations commonly required in seismic tape processing. Ungapped data records of any length may be read or written by the controller. Data Chaining is enabled on the SPECTRA 26T by closing switch 4 of the CPU Option Switch in location 10P. The SPECTRA 26T also supports triple density (800, 1600, and 6250 bpi) tape drives.

When data chaining is enabled on the SPECTRA 26T, four bits in the TPCS Control Words serve different purposes than under normal circumstances. These bits are described below.

CHAIN FLAG (Word 5, bit 15)

Software sets this bit to signal the controller that the current memory address is to be followed by a next memory buffer address. Data Chaining is therefore enabled.

BUFFER COMPLETE STATUS (Word 7, bit 4)

The controller sets this bit to indicate that it is ready to accept the next buffer address and character count.

GCR SELECT (Word 7, bit 5)

This bit selects 6250 bpi density, overriding Word 7, bit 6.

PE/NRZ SELECT (Word 7, bit 6)

When set, this bit selects PE (1600 bpi). When reset, this bit selects NRZ (800 bpi).

The chaining operation is initiated by the software setting the CHAIN FLAG (Word 5, bit 15) concurrently with the 15 LSBs of the memory buffer address. When the Control Words have been accepted, the controller sets IDLE (Word 7, bit 0) and BUFFER COMPLETE (Word 7, bit 4), then proceeds with data transfer. The software then examines Word 7 and terminates if the status shows an ERROR (Word 7, bit 2) or OPERATION COMPLETE (Word 7, bit 1). If the CHAIN FLAG was set, the software must update the Control Words (next buffer address, character count) and reset BUFFER COMPLETE. The controller waits for BUFFER COMPLETE to be cleared, and then proceeds with the next command in the chain. Upon completion of each data transfer, the controller checks to see if the CHAIN FLAG was set. If it was not, the controller sets OPERATION COMPLETE and terminates normally. If it was set, the controller continues with the next command.

NOTE: The character count (Word 4) must be even on all chained commands except the last one. The final command (CHAIN FLAG = 0) may have either an even or odd character count.

APPENDIX C

DRIVE CONFIGURATION TABLE

This section is intended to show which version of the SPECTRA 16/26 supports which drive. There are three mixed drive configurations included in the standard versions of the SPECTRA 16/26. These are:

1. 80MB & 300MB Drives
Versions A,B,C,M support a mixture of (3) 80MB drives with (1) 300 MB drive or (3) 300 MB drives with (1) 80MB drive
2. 80MB & 160MB Drives
Versions B,M supports a mixture of (2) 80MB drives with (1) 160MB drive mapped as 2 logical 80MB drives.
3. 300MB & 675MB Drives
Version B supports a mixture of (2) 300MB drives with (1) 675MB CDC FMD mapped as 2 logical 300MB drives. This is in fact the only standard configuration that supports the 675MB CDC FMD.

The following table is an attempt to list all major SMD compatible disk drives and to show which version of the SPECTRA 16/26 supports each drive. If a drive is not called out in this table it will be supported provided its parameters exactly match any drive that is in the table and is supported. For any other drives and for those drives in the table shown as not currently supported, they may be included in one of the current configurations or in a new one by request to Spectra Logic.

Type	Capacity	Spectra 16/26 Version	Notes
<u>Ampex</u>			
DM940	40 MB	A	64 Sectors
DM980	80 MB	A,B,C	61 or 64 Sectors in all versions
		M	56 Sectors
DM9160	160 MB	B	64 Sectors
DM9300	300 MB	A,B,C	61 Sectors in all versions
DM930A	300 MB	A,B,C	61 or 64 Sectors in all versions
		M	56 Sectors
DFR932	16/16 MB	A	64 Sectors mapped as 2 logical drives
		M	56 Sectors mapped as 2 logical drives
DFR964	16/48 MB	A	64 Sectors mapped as 2 logical drives
		A	64 Sectors mapped as 4 logical drives
		M	56 Sectors mapped as 2 logical drives
		M	56 Sectors mapped as 4 logical drives
DFR996	16/80 MB	A	64 Sectors mapped as 2 logical drives
		M	56 Sectors mapped as 2 logical drives
330	330 MB	B	64 Sectors

APPENDIX C

DRIVE CONFIGURATION TABLE (cont.)

Type	Capacity	Spectra 16/26 Version	Notes
<u>Fujitsu</u>			
2201	50 MB	None	
2211	80 MB	A,B,C M	61 or 64 Sectors in all versions 56 Sectors
2282	66 MB	None	
2283	132 MB	None	
2284	165 MB	B B M M	64 Sectors unmapped as 1 * 160 MB or 61 or 64 Sectors mapped as 2 * 80 MB 56 Sectors unmapped as 1 * 160 MB or 56 Sectors mapped as 2 * 80 MB
2294	330 MB	B	64 Sectors
2311	48 MB	None	
2312	84 MB	A,B,C M	64 Sectors in all versions 56 Sectors
2351	470 MB	B	88 Sectors mapped as 2 logical drives
<u>Kennedy</u>			
5300-70	70 MB	None	
5380	80 MB	A,B,C M	61 or 64 Sectors in all versions 56 Sectors
53160	160 MB	B,D B,D	64 Sectors unmapped as 1 * 160 MB or 61 or 64 Sectors mapped as 2 * 80 MB
7340	40 MB	A	64 Sectors
7380	80 MB	A,B,C	61 or 64 sectors in all versions
<u>Priam</u>			
3350	34 MB	C M	64 Sectors 56 Sectors
6650	67 MB	C M	64 Sectors 56 Sectors
15450	155 MB	C M	64 Sectors 56 Sectors
3450	35 MB	C	43 Sectors
7050	70 MB	C	43 Sectors
<u>Tecstor</u>			
160	160 MB	C	64 Sectors (700 cyls, 12 Heads)
165	165 MB	B,D B,D	61 or 64 Sectors mapped as 2 * 80 MB or 64 Sectors unmapped as 1 * 160 MB
315	315 MB	A,B,C M	61 or 64 Sectors in all versions 56 Sectors

APPENDIX C
DRIVE CONFIGURATION TABLE (cont.)

Type	Capacity	S16/26	Notes
<u>Ball</u> BD160	160 MB	B	64 Sectors
<u>Century Data</u> T82	80 MB	A,B,C,E M	61 or 64 Sectors in all versions 56 Sectors
T302	300 MB	A,B,C,N M	61 or 64 Sectors in all versions 56 Sectors
M80	80Mb	C	76 Sectors
M160	160 MB	C	101 Sectors
AMS190	190 MB	C	76 Sectors
AMS315	315 MB	A,B,C M	61 or 64 sectors in all versions 56 sectors
AMS380	380 MB	C	101 Sectors
AMS513	513 MB	C	101 Sectors
AMS571	571 MB	E	104 Sectors
<u>Control Data</u> SMD 9760	40 MB	A	64 Sectors
9762	80 MB	A,B,C,E M	61 or 64 Sectors in all versions 56 Sectors
9764	150 MB	None	
9766	300 MB	A,B,C,N M	61 or 64 Sectors in all versions 56 Sectors
CMD 9448-32	16/16 MB	A M	64 Sectors mapped as 2 logical drives 56 Sectors mapped as 2 logical drives
9448-64	16/48 MB	A A M M	64 Sectors mapped as 2 logical drives 64 Sectors mapped as 4 logical drives 56 Sectors mapped as 2 logical drives 56 Sectors mapped as 4 logical drives
9448-96	16/80 MB	A M	64 Sectors mapped as 2 logical drives 56 Sectors mapped as 2 logical drives
MMD 9730-12	12 MB	None	
9730-24	24 MB	None	
9730-80	80 MB	A,B,C,E M	61 or 64 Sectors in all versions 56 Sectors
9730-160	160 MB	B,D,N B,D M M	64 Sectors unmapped as 1 * 160 MB or 61 or 64 Sectors mapped as 2 * 80 MB 56 Sectors unmapped as 1 * 160 MB or 56 Sectors mapped as 2 * 80 MB
FMD 9775	675 MB	B	61 Sectors mapped as 2 * 300 MB
LARK 9455-16	8/8 MB	A	64 Sectors mapped as 2 logical drives
LARK 9455-50	25/25 MB	A,D	64 Sectors mapped as 2 logical drives
RSD 710	80 MB	A,B,C,E M	61 or 64 sectors in all versions 56 sectors
FSD 715	160 MB	B,D,N B,D M M	64 Sectors unmapped as 1 * 160 MB or 61 or 64 Sectors mapped as 2 * 80 MB 56 Sectors unmapped as 1 * 160 MB or 56 Sectors mapped as 2 * 80 MB
FSD 715	340 MB	N	64 Sectors
FSD 715	515 MB	N	95 Sectors
WINDSOR 9412-80	80 MB	D	64 Sectors
XMD	820 MB	D	128 Sectors

APPENDIX D SPECTRA 26T

In addition to performing standard tape operations, the SPECTRA 26T also supports data chaining operations commonly required in seismic tape processing. Ungapped data records of any length can be read or written by the controller. Data Chaining is enabled on the SPECTRA 26T by closing switch 4 of the CPU option switch in location 10P. The SPECTRA 26T also supports triple density (800, 1600, and 6250 BPI) tape drives.

When data chaining is enabled on the SPECTRA 26T, four bits in the TPCS control words serve different purposes than under normal circumstances. These bits are described below.

- WORD 5 BIT 15 - CHAIN FLAG
Software sets this bit to signal the controller that the current memory address is to be followed by a next memory buffer address. Data chaining is thus enabled.

- WORD 7 BIT 4 - BUFFER COMPLETE STATUS
The controller sets this bit to indicate that it is ready to accept the next buffer address and character count.

- WORD 7 BIT 5 - GCR SELECT
This bit selects 6250 BPI density, overrides WORD 7 BIT 6.

- WORD 7 BIT 6 - PE/NRZ SELECT
When set, this bit selects PE (1600 BPI). When reset, it selects NRZ (800 BPI).

Data Chaining, General Description

The chaining operation is initiated by the software setting the CHAIN FLAG (WORD 5, BIT 15) concurrently with the 15 LSB's of the memory buffer address. When the control words have been accepted, the controller sets IDLE (WORD 7, BIT 0) and BUFFER COMPLETE (WORD 7, BIT 4) and proceeds with data transfer. The software then examines WORD 7 and terminates if the status shows an ERROR (WORD 7, BIT 2) or OPERATION COMPLETE (WORD 7, BIT 1). If the CHAIN FLAG was set, the software must update the control words (next buffer address, character count) and reset BUFFER COMPLETE. The controller waits for BUFFER COMPLETE to be cleared, and then proceeds with the next command in the chain. Upon completion of each data transfer, the controller checks to see if the CHAIN FLAG was set. If it was not, the controller sets OPERATION COMPLETE and terminates normally. If it was set, the controller continues with the next command.

NOTE: The character count (WORD 4) must be even on all chained commands except the last one. The final command (CHAIN FLAG = 0) may have an even or odd character count.

RETURN INFORMATION REFERENCE SHEET



A DIVISION OF CIPHER DATA PRODUCTS, INC.

SPECTRA LOGIC
297 NORTH BERNARDO AVE.
P.O. BOX 7260
MOUNTAIN VIEW, CA.
94039-7260
(415)964-2211

IMPORTANT: This form should be completed **ONLY AFTER RETURN SHIPMENT HAS BEEN PRE-AUTHORIZED BY SPECTRA LOGIC.** Contact Customer Support Department for further information.

MODEL# _____
SERIAL# _____

COMPANY NAME: _____
CONTACT NAME: _____
PHONE#() _____

REASON FOR RETURN:
CREDIT _____
MARKETING DEMO _____
UPDATED ONLY _____
REPAIR _____

DATE _____ CRO# _____

IN WARRANTY _____
OUT OF WARRANTY _____

THE REMAINDER OF THIS FORM SHOULD BE COMPLETED ONLY IF REPAIR IS NEEDED.

Did the Controller Work Previously? _____ Or was it DOA? _____

CPU TYPE _____
OPERATING SYSTEM & REV. _____
DISK DRIVE MODEL(S) _____
TAPE DRIVE MODEL(S) _____

Other comments on System Configuration (i.e.-mapping?) _____

Did the board fail during diagnostics? _____
microdiagnostics? _____
or operating system? _____

If diagnostic was run, give diagnostic name and detailed error message, and/or attach hard copy. _____

Other Comments _____